Volume 5

MICROWAVE AND RF DESIGN

AMPLIFIERS AND OSCILLATORS

Michael Steer

Third Edition

Microwave and RF Design
Amplifiers and Oscillators

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To my Mother

Mary Elizabeth

Preface

The book series *Microwave and RF Design* is a comprehensive treatment of radio frequency (RF) and microwave design with a modern "systems-first" approach. A strong emphasis on design permeates the series with extensive case studies and design examples. Design is oriented towards cellular communications and microstrip design so that lessons learned can be applied to real-world design tasks. The books in the Microwave and RF Design series are:

- Microwave and RF Design: Radio Systems, Volume 1
- Microwave and RF Design: Transmission Lines, Volume 2
- Microwave and RF Design: Networks, Volume 3
- Microwave and RF Design: Modules, Volume 4
- Microwave and RF Design: Amplifiers and Oscillators, Volume 5

The length and format of each is suitable for automatic printing and binding.

Rationale

The central philosophy behind this series's popular approach is that the student or practicing engineer will develop a full appreciation for RF and microwave engineering and gain the practical skills to perform system-level design decisions. Now more than ever companies need engineers with an ingrained appreciation of systems and armed with the skills to make system decisions. One of the greatest challenges facing RF and microwave engineering is the increasing level of abstraction needed to create innovative microwave and RF systems. This book series is organized in such a way that the reader comes to understand the impact that system-level decisions have on component and subsystem design. At the same time, the capabilities of technologies, components, and subsystems impact system design. The book series is meticulously crafted to intertwine these themes.

Audience

The book series was originally developed for three courses at North Carolina State University. One is a final-year undergraduate class, another an introductory graduate class, and the third an advanced graduate class. Books in the series are used as supplementary texts in two other classes. There are extensive case studies, examples, and end of chapter problems ranging from straight-forward to in-depth problems requiring hours to solve. A companion book, *Fundamentals of Microwave and RF Design*, is more suitable for an undergraduate class yet there is a direct linkage between the material in this book and the series which can then be used as a career-long reference text. I believe it is completely understandable for senior-level students where a microwave/RF engineering course is offered. The book series is a comprehensive RF and microwave text and reference, with detailed index, appendices, and cross-references throughout. Practicing engineers will find the book series a valuable systems primer, a refresher as needed, and a

reference tool in the field. Additionally, it can serve as a valuable, accessible resource for those outside RF circuit engineering who need to understand how they can work with RF hardware engineers.

Organization

This book is a volume in a five volume series on RF and microwave design. The first volume in the series, *Microwave and RF Design: Radio Systems*, addresses radio systems mainly following the evolution of cellular radio. A central aspect of microwave engineering is distributed effects considered in the second volume of this book series, *Microwave and RF Design: Transmission Lines*. Here transmission lines are treated as supporting forward- and backward-traveling voltage and current waves and these are related to electromagnetic effects. The third volume, *Microwave and RF Design: Networks*, covers microwave network theory which is the theory that describes power flow and can be used with transmission line effects. Topics covered in *Microwave and RF Design: Modules*, focus on designing microwave circuits and systems using modules introducing a large number of different modules. Modules is just another term for a network but the implication is that is is packaged and often available off-the-shelf. Other topics that are important in system design using modules are considered including noise, distortion, and dynamic range. Most microwave and RF designers construct systems using modules developed by other engineers who specialize in developing the modules. Examples are filter and amplifier modules which once designed can be used in many different systems. Much of microwave design is about maximizing dynamic range, minimizing noise, and minimizing DC power consumption. The fifth volume in this series, *Microwave and RF Design: Amplifiers and Oscillators*, considers amplifier and oscillator design and develops the skills required to develop modules.

Volume 1: Microwave and RF Design: Radio Systems

The first book of the series covers RF systems. It describes system concepts and provides comprehensive knowledge of RF and microwave systems. The emphasis is on understanding how systems are crafted from many different technologies and concepts. The reader gains valuable insight into how different technologies can be traded off in meeting system requirements. I do not believe this systems presentation is available anywhere else in such a compact form.

Volume 2: Microwave and RF Design: Transmission Lines

This book begins with a chapter on transmission line theory and introduces the concepts of forward- and backward-traveling waves. Many examples are included of advanced techniques for analyzing and designing transmission line networks. This is followed by a chapter on planar transmission lines with microstrip lines primarily used in design examples. Design examples illustrate some of the less quantifiable design decisions that must be made. The next chapter describes frequency-dependent transmission line effects and describes the design choices that must be taken to avoid multimoding. The final chapter in this volume addresses coupled-lines. It is shown how to design coupled-line networks that exploit this distributed effect to realize novel circuit functionality and how to design networks that minimize negative effects. The modern treatment of transmission lines in this volume emphasizes planar circuit design and the practical aspects of designing

around unwanted effects. Detailed design of a directional coupler is used to illustrate the use of coupled lines. Network equivalents of coupled lines are introduced as fundamental building blocks that are used later in the synthesis of coupled-line filters. The text, examples, and problems introduce the often hidden design requirements of designing to mitigate parasitic effects and unwanted modes of operation.

Volume 3: Microwave and RF Design: Networks

Volume 3 focuses on microwave networks with descriptions based on S parameters and $ABCD$ matrices, and the representation of reflection and transmission information on polar plots called Smith charts. Microwave measurement and calibration technology are examined. A sampling of the wide variety of microwave elements based on transmission lines is presented. It is shown how many of these have lumped-element equivalents and how lumped elements and transmission lines can be combined as a compromise between the high performance of transmission line structures and the compactness of lumped elements. This volume concludes with an in-depth treatment of matching for maximum power transfer. Both lumped-element and distributed-element matching are presented.

Volume 4: Microwave and RF Design: Modules

Volume 4 focuses on the design of systems based on microwave modules. The book considers the wide variety of RF modules including amplifiers, local oscillators, switches, circulators, isolators, phase detectors, frequency multipliers and dividers, phase-locked loops, and direct digital synthesizers. The use of modules has become increasingly important in RF and microwave engineering. A wide variety of passive and active modules are available and high-performance systems can be realized cost effectively and with stellar performance by using off-the-shelf modules interconnected using planar transmission lines. Module vendors are encouraged by the market to develop competitive modules that can be used in a wide variety of applications. The great majority of RF and microwave engineers either develop modules or use modules to realize RF systems. Systems must also be concerned with noise and distortion, including distortion that originates in supposedly linear elements. Something as simple as a termination can produce distortion called passive intermodulation distortion. Design techniques are presented for designing cascaded systems while managing noise and distortion. Filters are also modules and general filter theory is covered and the design of parallel coupled line filters is presented in detail. Filter design is presented as a mixture of art and science. This mix, and the thought processes involved, are emphasized through the design of a filter integrated throughout this chapter.

Volume 5: Microwave and RF Design: Amplifiers and Oscillators

The fifth volume presents the design of amplifiers and oscillators in a way that enables state-of-the-art designs to be developed. Detailed strategies for amplifiers and voltage-controlled oscillators are presented. Design of competitive microwave amplifiers and oscillators are particularly challenging as many trade-offs are required in design, and the design decisions cannot be reduced to a formulaic flow. Very detailed case studies are presented and while some may seem quite complicated, they parallel the level of sophistication required to develop competitive designs.

Case Studies

A key feature of this book series is the use of real world case studies of leading edge designs. Some of the case studies are designs done in my research group to demonstrate design techniques resulting in leading performance. The case studies and the persons responsible for helping to develop them are as follows.

1. Software defined radio transmitter.
2. High dynamic range down converter design. This case study was developed with Alan Victor.
3. Design of a third-order Chebyshev combline filter. This case study was developed with Wael Fathelbab.
4. Design of a bandstop filter. This case study was developed with Wael Fathelbab.
5. Tunable Resonator with a varactor diode stack. This case study was developed with Alan Victor.
6. Analysis of a 15 GHz Receiver. This case study was developed with Alan Victor.
7. Transceiver Architecture. This case study was developed with Alan Victor.
8. Narrowband linear amplifier design. This case study was developed with Dane Collins and National Instruments Corporation.
9. Wideband Amplifier Design. This case study was developed with Dane Collins and National Instruments Corporation.
10. Distributed biasing of differential amplifiers. This case study was developed with Wael Fathelbab.
11. Analysis of a distributed amplifier. This case study was developed with Ratan Bhatia, Jason Gerber, Tony Kwan, and Rowan Gilmore.
12. Design of a WiMAX power amplifier. This case study was developed with Dane Collins and National Instruments Corporation.
13. Reflection oscillator. This case study was developed with Dane Collins and National Instruments Corporation.
14. Design of a C-Band VCO. This case study was developed with Alan Victor.
15. Oscillator phase noise analysis. This case study was developed with Dane Collins and National Instruments Corporation.

Many of these case studies are available as captioned YouTube videos and qualified instructors can request higher resolution videos from the author.

Course Structures

Based on the adoption of the first and second editions at universities, several different university courses have been developed using various parts of what was originally one very large book. The book supports teaching two or three classes with courses varying by the selection of volumes and chapters. A standard microwave class following the format of earlier microwave texts can be taught using the second and third volumes. Such a course will benefit from the strong practical design flavor and modern treatment of measurement technology, Smith charts, and matching networks. Transmission line propagation and design is presented in the context of microstrip technology providing an immediately useful skill. The subtleties of multimoding are also presented in the context of microstrip lines. In such

a class the first volume on microwave systems can be assigned for self-learning.

Another approach is to teach a course that focuses on transmission line effects including parallel coupled-line filters and module design. Such a class would focus on Volumes 2, 3 and 4. A filter design course would focus on using Volume 4 on module design. A course on amplifier and oscillator design would use Volume 5. This course is supported by a large number of case studies that present design concepts that would otherwise be difficult to put into the flow of the textbook.

Another option suited to an undergraduate or introductory graduate class is to teach a class that enables engineers to develop RF and microwave systems. This class uses portions of Volumes 2, 3 and 4. This class then omits detailed filter, amplifier, and oscillator design.

The fundamental philosophy behind the book series is that the broader impact of the material should be presented first. Systems should be discussed up front and not left as an afterthought for the final chapter of a textbook, the last lecture of the semester, or the last course of a curriculum.

The book series is written so that all electrical engineers can gain an appreciation of RF and microwave hardware engineering. The body of the text can be covered without strong reliance on this electromagnetic theory, but it is there for those who desire it for teaching or reader review. The book is rich with detailed information and also serves as a technical reference.

The Systems Engineer

Systems are developed beginning with fuzzy requirements for components and subsystems. Just as system requirements provide impetus to develop new base technologies, the development of new technologies provides new capabilities that drive innovation and new systems. The new capabilities may arise from developments made in support of other systems. Sometimes serendipity leads to the new capabilities. Creating innovative microwave and RF systems that address market needs or provide for new opportunities is the most exciting challenge in RF design. The engineers who can conceptualize and architect new RF systems are in great demand. This book began as an effort to train RF systems engineers and as an RF systems resource for practicing engineers. Many RF systems engineers began their careers when systems were simple. Today, appreciating a system requires higher levels of abstraction than in the past, but it also requires detailed knowledge or the ability to access detailed knowledge and expertise. So what makes a systems engineer? There is not a simple answer, but many partial answers. We know that system engineers have great technical confidence and broad appreciation for technologies. They are both broad in their knowledge of a large swath of technologies and also deep in knowledge of a few areas, sometimes called the “T” model. One book or course will not make a systems engineer. It is clear that there must be a diverse set of experiences. This book series fulfills the role of fostering both high-level abstraction of RF engineering and also detailed design skills to realize effective RF and microwave modules. My hope is that this book will provide the necessary background for the next generation of RF systems engineers by stressing system principles immediately, followed by core RF technologies. Core technologies are thereby covered within the context of the systems in which they are used.

Supplementary Materials

Supplementary materials available to qualified instructors adopting the book include PowerPoint slides and solutions to the end-of-chapter problems. Requests should be directed to the author. Access to downloads of the books, additional material and YouTube videos of many case studies are available at https://www.lib.ncsu.edu/do/open-education

Acknowledgments

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The book was produced using LaTeX and open access fonts, line art was drawn using xfig and inkscape, and images were edited in gimp. So thanks to the many volunteers who developed these packages.

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CHAPTER 1

Introduction to Active RF and Microwave Circuits

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1.1 Introduction to Amplifiers and Oscillators

Design of microwave amplifiers and oscillators is the most challenging of microwave designs determining the performance and DC power consumption of microwave systems. Most of the challenges arise because of the capacitive parasitics of microwave transistors and also because some types of transistors, such as silicon transistors, have quite low intrinsic power gain. Packaged transistors which are used in hybrid design and design using modules have the additional complexity of package inductance as well as additional capacitance from the package. With amplifiers one of the great challenges is achieving wide bandwidth so that the same amplifier can be used for multiple frequency bands. For example, with cellular communications it is desirable if one amplifier could be used for multiple cellular bands. However most of the time a cellular system handset must have different transmit and receive amplifiers for each of the cellular bands. The transistor's capacitive, and if packaged inductive, parasitics determine the minimum Q and thus maximum bandwidth. The matching required to interface the input and the of an amplifier output of transistors can only further reduce bandwidth.

Microwave amplifier design generally uses the topology shown in Figure 1-1 with the transistor biased in a high-gain region and the input and output matching networks used to provide good power transfer at the input and output of the transistors. The DC bias control circuit is fairly standard; it does not involve any microwave constraints other than the need to block RF currents from the bias circuit. The lowpass filters (in the bias circuits) can have one of several forms and are often integrated into the input and output matching networks. Synthesis of the input and output matching networks (and occasionally a feedback network required for stability and broadband operation) is the primary objective of any amplifier design.

Design of linear microwave amplifiers where narrowband operation is

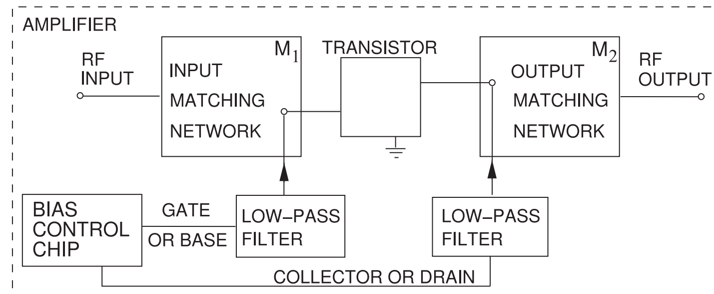

Figure 1-1: Block diagram of an RF amplifier including biasing networks.

sufficient is considered in Chapter 2 where the topology shown in Figure 1-1 is nearly always followed. The input and output matching networks limit the bandwidth of the amplifier and are ideally lossless. This chapter develops the skills required to trade off gain, noise, and stability. These trade-offs are required with all types of microwave amplifier design. The chapter presents a case study of narrowband linear amplifier design.

Chapter 3 presents strategies for designing a wideband amplifier and again the topology shown in Figure 1-1 is usually followed. Wideband is still limited as usually the best that can be achieved for an efficient amplifier is a bandwidth of only half-an-octave such as a bandwidth from 2 to 3 GHz. Sometimes there is inductive and capacitive feedback around the transistor to compensate for the inherent gain roll-off with respect to frequency of transistors, especially FETs. The chapter includes a case study on the design of a wideband amplifier. A case study is a good way to present design methods as it enables design decisions to be discussed. Rarely can design decisions be reduced to a formulaic flow. One of the important trade-offs is trading off gain and noise performance and in the case study it will be seen how this can be done graphically. A distributed amplifier is one type of amplifiers that has a very wide bandwidth, perhaps 2–4 octaves, e.g. 2 to 4 GHz or 2 to 16 GHz, but has an efficiency of only a few percent. The topology differs significantly from the input and output matching network–based topology of Figure 1-1. The distributed amplifier achieves wide bandwidth by incorporating the parasitics of multiple transistors in a transmission line where the input and output capacitances of transistors augment the capacitances in the LC model of an actual transmission line. A case study is presented that analyses a distributed amplifier. Efficient biasing of a wideband amplifier can be a challenge and a final case study presents a technique for distributed biasing of a differential amplifier.

The fourth chapter considers power amplifiers where the emphasis is on producing large powers at high efficiency and bandwidth is sacrificed. Usually at high powers efficiencies are achieved by engineering the transistor's current and voltage waveforms by manipulating the impedances presented at harmonics. This is the source of the low bandwidth. A case study of the design of a WiMAX power amplifier is undertaken.

The final chapter of this book considers the design of microwave oscillators. Microwave oscillator design is particularly challenging. Oscillators consume considerable DC power and are a competitive differentiator. There are two quite different classes of design, one for oscillators that are fixed in frequency and one for the much more useful voltage-controlled oscillator which has variable frequency. Case studies are presented for each of these two types of oscillators.

The remainder of this current chapter describes transistor technology and an appendix describes particular models of transistors that are used in circuit simulators. Today's simulators use transistor models that are very sophisticated compared to those models described in the appendix, however they are not amenable to developing a designer's intuition. The simpler models considered in the appendix, state-of-the-art models from 20 and 30 years ago, provide the desired intuition for a designer.

1.2 Book Outline

This book is the fifth volume in a series on microwave and RF design. The first volume in the series addresses radio systems [1] mainly following the evolution of cellular radio. A central aspect of microwave engineering is distributed effects considered in the second volume of his book series [2]. Here transmission lines are treated as supporting forward- and backward-traveling voltage and current waves and these are related to electromagnetic effects. The third volume [3] covers microwave network theory which is the theory that describes power flow and can be used with transmission line effects. Topics covered in this volume include scattering parameters, Smith charts, and matching networks that enable maximum power transfer. The fourth volume [4] focuses on designing microwave circuits and systems using modules introducing a large number of different modules. Modules is just another term for a network but the implication is that is is packaged and often available off-the-shelf. Other topics in this chapter that are important in system design using modules are considered including noise, distortion, and dynamic range. Most microwave and RF designers construct systems using modules developed by other engineers who specialize in developing the modules. Examples are filter and amplifier chip modules which once designed can be used in many different systems. Much of microwave design is about maximizing dynamic range, minimizing noise, and minimizing DC power consumption.

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- Microwave and RF Design: Transmission Lines
- Microwave and RF Design: Networks
- Microwave and RF Design: Modules
- Microwave and RF Design: Amplifiers and Oscillators

1.3 Transistor Technology

Transistors are semiconductor devices with three (and sometimes more) terminals. The third terminal enables output current to be controlled by a relatively small and low-power input signal. In amplifiers, transistors are used to achieve current gain, voltage gain, or power gain. Most often power gain is the objective in RF and microwave design. Most transistors are fabricated using silicon (Si) or **compound semiconductors** such as **gallium-arsenide** (**GaAs**), **indium phosphide** (**InP**), or **gallium-nitride** (**GaN**). The overwhelming trend is to use silicon technology because of the much higher integration density that is possible, with compound semiconductor technology used only when it provides a unique advantage such as high power, superior noise performance, or high efficiency. Germanium is used

as a dopant in silicon and then silicon is referred to as silicon germanium but usually germanium is in a very small proportion to silicon so SiGe as described here is silicon with a dopant. With comparable concentrations of silicon and germanium SiGe is a compound semiconductor and this is used as a compound semiconductor at times.

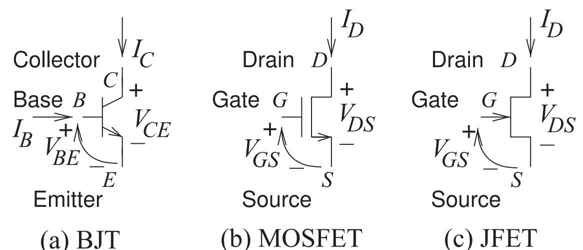
There are three fundamental types of microwave transistors [5, 6]: **bipolar junction transistors**, (**BJTs**); **junction field effect transistors**, (**JFETs**); and **insulated gate FETs**, (**IGFETs**), with the **metal-oxide-semiconductor FETs**, (**MOSFETs**), being the most common type of IGFET. The schematics and terminal definitions of the three fundamental types of transistors are shown in Figure 1-2. The three fundamental types of transistors are considered in the following subsections.

1.3.1 BJT and HBT Fundamentals

A bipolar transistor has three semiconductor regions called the collector (C), base (B), and emitter (E), as shown in the BJT cross section of Figure 1-3(a). An npn BJT has n-type semiconductor at the emitter and collector, and p-type semiconductor forms the base. In this transistor, the positive sense of current flow is from the collector through the base to the emitter (see Figure 1-3(a)) and the dominant carriers in the p-type base region are electrons, and so this is called a **minority carrier device**. The collector current is dependent on the number of carriers injected into the base region from the base terminal. In a pnp BJT the collector, base, and emitter are p-type, n-type, and p-type, respectively, and the majority carriers in the base are holes. Current flow is then from the emitter through the base to the collector. If the base region is thin and the emitter is doped at a higher concentration than the base, then the collector current, I_C, is much greater than I_B, with $I_C = \beta_F I_B$, where β_F is called the forward current gain and commonly has a value of several hundred. The key to high performance is a thin base region.

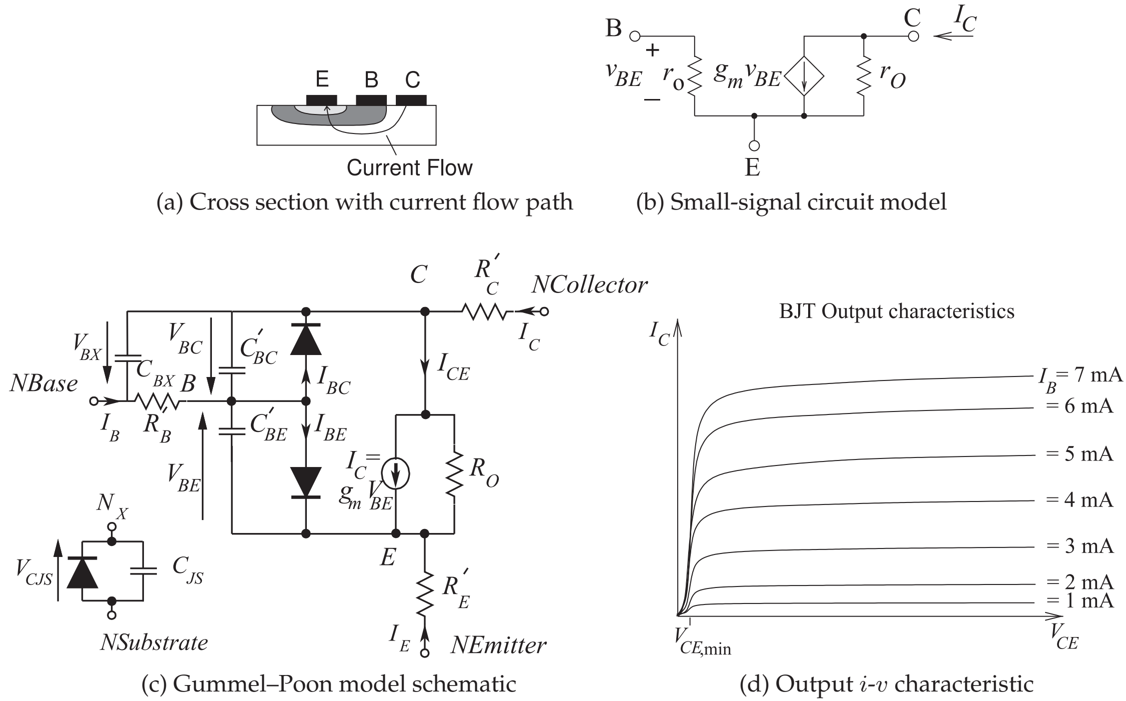
When realized in silicon, a bipolar transistor is called a bipolar junction transistor, (BJT); and in compound semiconductor technology it is a **heterostructure bipolar transistor**, (**HBT**). In a silicon germanium (SiGe) BJT transistor, germanium is normally used to increase the hole and electron mobility and the device is not regarded as a compound semiconductor transistor.

The fundamental operation of a BJT transistor was described by Gummel and Poon [7] using equations that are now implemented in circuit simulators and known as the Gummel–Poon model. The circuit schematic of the Gummel–Poon model is shown in Figure 1-3(c). It is the basis for more



(a) BJT (b) MOSFET (c) JFET

Figure 1-2: Transistor schematics: (a) pnp bipolar transistor with B for the base terminal, C for the collector terminal, and E for the emitter terminal; (b) n-type MOSFET (nMOS); and (c) n-type JFET (nJFET) with G for the gate terminal, D for the drain terminal, and S for the source terminal. The schematic symbol for a BJT is used for HBTs; and the schematic symbol for a JFET is used for MESFETs, HEMTS, and pHEMTs.



(a) Cross section with current flow path (b) Small-signal circuit model

(c) Gummel–Poon model schematic (d) Output i-v characteristic

Figure 1-3: BJT details.

sophisticated BJT and HBT models that capture parasitic and other second-order effects. Both hole and electron charge carriers are involved in current conduction, hence the term bipolar. The Gummel–Poon model is described in Section 1.A.3 and the fundamental operation is described by Equations (1.72)–(1.82). Summarizing, the base-emitter current is

$$I_{BE} = I_{BF}/\beta_F + I_{LE} \tag{1.1}$$

and the base-collector current is

$$I_{BC} = I_{BR}/\beta_R + I_{LC}, \tag{1.2}$$

where β_R is the reverse current gain. The collector-emitter current is

$$I_{CE} = I_{BF} - I_{BR}/K_{QB}. \tag{1.3}$$

The forward diffusion current is

$$I_{BF} = I_S \left(\mathrm{e}^{V_{BE}/(N_F V_{TH})} - 1 \right), \tag{1.4}$$

the nonideal base-emitter current is

$$I_{LE} = I_{SE} \left(\mathrm{e}^{V_{BE}/(N_E V_{TH})} - 1 \right), \tag{1.5}$$

the reverse diffusion current is

$$I_{BR} = I_S \left(\mathrm{e}^{V_{BC}/(N_R V_{TH})} - 1 \right), \tag{1.6}$$

the nonideal base-collector current is

$$I_{LC} = I_{SC}\left(e^{V_{BC}/(N_C V_{TH})} - 1\right), \quad (1.7)$$

and the base charge factor is

$$K_{QB} = \frac{1}{2}\left[1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AB}}\right]^{-1}\left[1 + \sqrt{1 + 4\left(\frac{I_{BF}}{I_{KF}} + \frac{I_{BR}}{I_{KR}}\right)}\right]. \quad (1.8)$$

Thus the conductive current flowing into the base is

$$I_B = I_{BE} + I_{BC}, \quad (1.9)$$

the conductive current flowing into the collector is

$$I_C = I_{CE} - I_{BC}, \quad (1.10)$$

and the conductive current flowing into the emitter is

$$I_E = I_{BE} + I_{CE}. \quad (1.11)$$

The forward current gain, β_F, is much greater than the reverse current gain, β_R, and the nonideal base-emitter and base-collector currents are small. Equations (1.1)–(1.11) can then be reduced so that the base current is approximately

$$I_B = \frac{I_S}{\beta_F}\left(e^{V_{BE}/(N_F V_{TH})} - 1\right), \quad (1.12)$$

the conductive current flowing into the collector is

$$I_C = \beta_F I_B, \quad (1.13)$$

and the conductive current flowing into the emitter is

$$I_E = I_B + I_C. \quad (1.14)$$

From Equations (1.12) and (1.13) it is seen that the fundamental operation of a BJT is as a voltage-controlled current source. This leads to the small-signal circuit model of a BJT, biased in its fundamental mode of operation, shown in Figure 1-3(b).

The schematic symbols used for BJTs are shown in Table 1-1 with the arrow pointing to the n-type semiconductor. The BJT symbol is also the symbol for a HBT.

1.3.2 MOSFET Fundamentals

There are several types of FETs, with the MOSFET being the most common. With all FETs there is a channel between two terminals, the source and drain, and an applied field produced by a voltage at a third terminal, the gate, controls the cross section of the channel and the number of carriers in the channel. Hence the gate voltage controls the current flow between the drain and the source. With some FETs, the channel does not exist until a gate field is applied and pulls carriers from the bulk into the channel, and this

Transistor	IEEE symbol	Commonly used symbol
BJT, pnp	B E C	B E C
BJT, npn	B C E	B C E

Table 1-1: IEEE standard schematic symbols for bipolar junction transistors (BJTs and HBTs) [8] and commonly used symbols in layouts [9]. The letters indicate terminals: B (base), C (collector), E (emitter). These symbols are used for silicon BJTs and compound semiconductor HBTs.

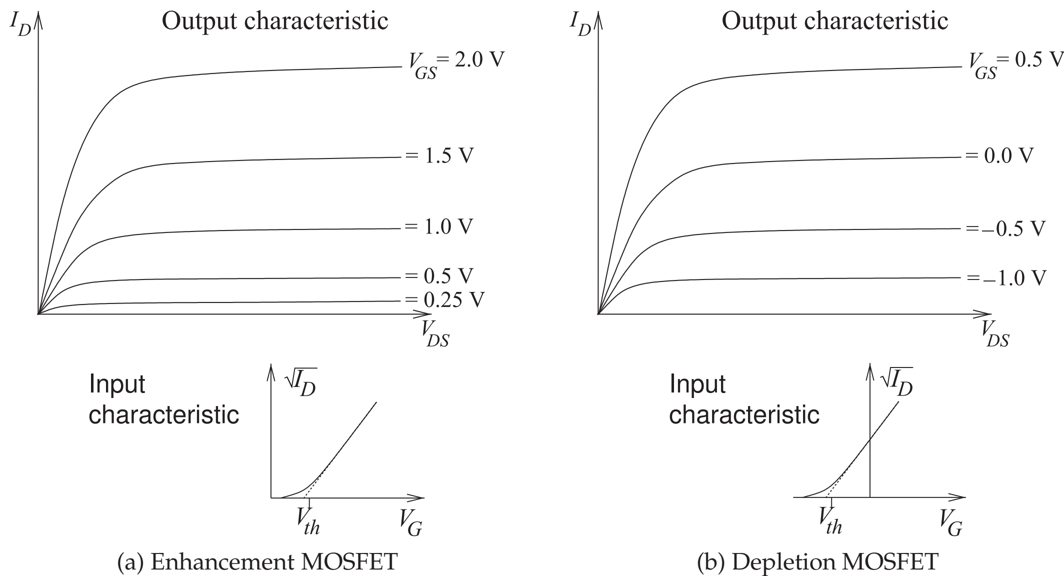


Figure 1-4: Current-voltage characteristics of depletion- and enhancement-mode MOSFETs.

is called an **enhancement-mode** FET. The input and output characteristics of the enhancement-mode FET are shown in Figure 1-4(a). With some MOSFETs with a particular doping profile, carriers are in the channel even without an applied field and a gate voltage either enhances the cross section of the channel or closes it off. Most often the gate voltage is used to reduce current conduction, and this type of FET is called a **depletion-mode** FET. The input and output characteristics of the depletion-mode FET are shown in Figure 1-4(b). The enhancement-mode MOSFET is much more common than the depletion-mode.

The enhancement MOSFET is a relatively simple device to fabricate and is the smallest of the semiconductor transistors. It is the preferred technology for high-density integration. The three-dimensional view and cross sections of a MOSFET are shown in Figure 1-5(a–c). The cross-section of an nMOS transistor is shown in Figure 1-5(b) where there is a p-type substrate and an n-type channel is created when there is sufficient voltage at the gate. As well as the source and drain connection, there is a fourth terminal call the body connection denoted as U in Figure 1-5(b) but B is also used and this can be confused with the base of a BJT transistor. The body is typically

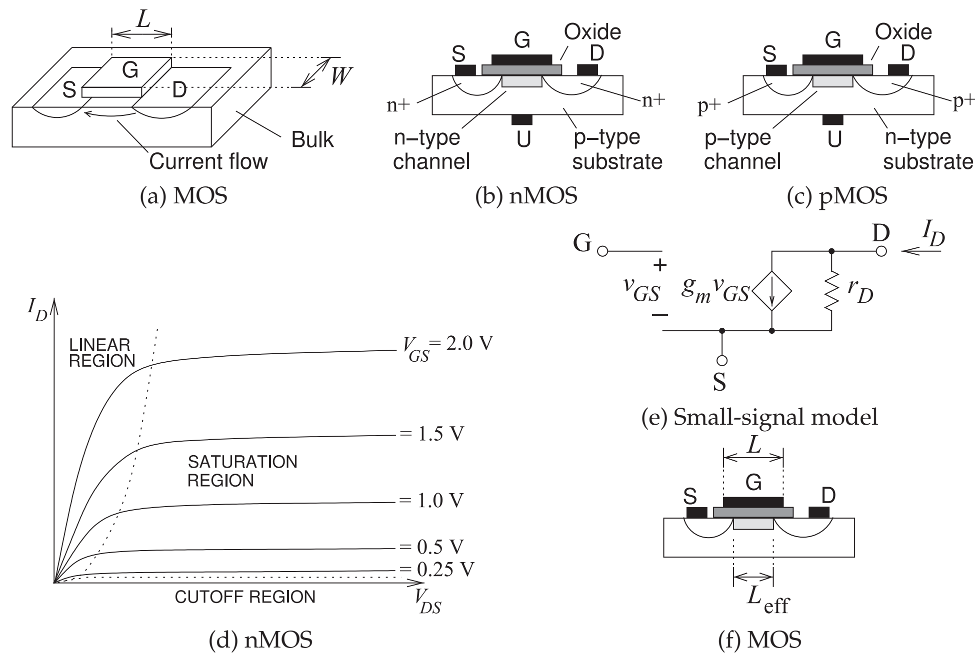


Figure 1-5: MOSFET details: (a) three-dimensional view of a MOSFET; (b) cross section of an nMOS transistor with metal or **polysilicon** contacts indicated by the black blocks; (c)the corresponding cross section of a pMOS transistor; (d) current-voltage characteristics of an enhancement-mode MOSFET; (e) circuit model of fundamental operation; and (f) cross section showing the effective gate length, $L_{\rm EFF}$. The **linear region** is sometimes (but less often) called the **triode region** because of similarity to the characteristics of the triode vacuum tube device. Similarly the **saturation region** is sometimes called the **pentode region**.

connected to the most negative voltage in the circuit so that the substrate-to-channel interface is a reverse-biased diode. A similar situation occurs with the pMOS transistor with the cross-section of Figure 1-5(c). Now there is a p-type channel and an n-type substrate so that the body (U) must typically be connected to the most positive voltage in the circuit to ensure a reverse-biased junction between the substrate and the channel.

A MOSFET has metal or polysilicon (a reasonable conductor [5, 6, 10]) connections at the drain (D), source (S) and gate (G). The MOSFET is nearly always silicon, but possibly (**GaN!MOSFET** [11, 12]. The source and drain connections are highly doped (n+ for nMOS and p+ for pMOS) semiconductor regions providing a good ohmic contact rather than forming a Schottky barrier.[1] The gate is not in direct contact with the semiconductor, but separated by a thin layer of oxide. With no voltage applied at the gate, there are no carriers below the gate oxide that can conduct current between the source and drain. A gate voltage is necessary to draw carriers to the channel region, forming a conducting channel. That is, a voltage applied to the gate creates an electric field that induces electrons (the n carriers for

[1] A Schottky barrier occurs at the abrupt interface between a metal and a doped semiconductor.

an nMOSFET) to form a conducting channel immediately under the oxide.[2] This process is called inversion. The length of the channel is denoted $L_{\rm eff}$ (the effective gate length), which is less than the actual gate length L as the highly doped source and drain regions must extend under the gate to ensure good contact to the induced channel. This is indicated in Figure 1-5(e). The number of carriers in the channel is controlled by the gate voltage. A higher frequency of operation is obtained by reducing $L_{\rm eff}$.

Three distinct regions of operation, identified in Figure 1-5(d), are recognized for a MOSFET. In the linear region the drain-source current, I_{DS}, continues to increase as the drain-source voltage, V_{DS}, increases. I_{DS} depends on both the drain-source and gate-source voltage, V_{DS} and V_{GS}, so the linear region is sometimes exploited in mixers. In the saturation region, I_{DS} is almost independent of V_{DS} and almost solely controlled by V_{GS}. MOSFET amplifiers operate in the saturation region. The cutoff region is when there is negligible drain current, and a FET is particularly effective at shutting off conduction and so makes a good voltage-controlled switch.

In initial design the mode of fundamental operation must be intuitively understood and simple models and equations are needed. In contrast, a circuit simulator requires a detailed model capturing subtle physical effects. A model of a MOSFET that can be used in a circuit simulator is presented in Section 1.A.1. The model presented is known as the Level 3 MOSFET model and captures the fundamental operation of MOSFETs as well as capacitive parasitic effects. Models are developed using physical insight into semiconductor operation. All semiconductor device models, not just MOSFETs, require extensive fitting to measured data and have limited accuracy. Consequently the design, fabrication, and test cycle are critically important to realizing transistor circuits.

In the saturation region (see Figure 1-5(d)) the fundamental operation of a MOSFET is described by Equation (1.47), which is repeated here:

$$I_{DS} = \frac{W_{\rm eff}}{L_{\rm eff}}\,\mu_{\rm eff}\,C_{ox}\left[(V_{GS}-V_{th}) - 1 + \frac{F_B}{2}\,V_{d\rm sat}\right]V_{d\rm sat}. \tag{1.15}$$

Here C_{ox} is the capacitance of the gate oxide, $W_{\rm eff}$ is the effective gate width, which is the gate width W modified by fringing and related effects, V_{th} is the **threshold voltage**, and $\mu_{\rm eff}$ is the effective mobility[3] of the carriers in the channel (electrons for an nMOSFET and holes for a pMOSFET). $V_{d\rm sat}$ is the drain saturation voltage and is the drain source voltage at which the device enters the saturation region from the linear region. F_B is due to the charge in the bulk semiconductor (below the channel) on which the gate-induced electric field terminates. $L_{\rm eff}$ is the effective gate length and this is modulated by the drain-source voltage so that [5, 6, 10]

$$L_{\rm eff} = \frac{L}{1+\lambda V_{DS}}. \tag{1.16}$$

Accounting for channel length modulation, described by Equation (1.16),

---

[2] The discussion is similar for a pMOSFET, but with holes (p-type carriers) forming the channel.

[3] **Mobility**, μ, is the proportionality of the velocity of carriers to the applied electric field, $v_d = \mu E$, where v_d is the average drift velocity of carriers and E is the applied electric field. Mobility has the units $\mathrm{m^2/(V\cdot s)}$, i.e. $\mathrm{m^2\cdot V^{-1}\cdot s^{-1}}$.

and simplifying [5, 6, 10], Equation (1.15) becomes

$$I_{DS} = \frac{W}{L}\frac{\mu_{\text{eff}} C_{ox}}{2}\left(V_{GS} - V_{th}\right)^2 \left(1 + \lambda V_{DS}\right). \tag{1.17}$$

This equation embodies the fundamental operation needed in developing initial designs. The key is that the MOSFET can be modeled (at least in the saturation region) as a voltage-controlled current source as shown in the model of Figure 1-5(e). The transconductance, g_m (in saturation), is obtained by differentiating Equation (1.17) so that (ignoring channel length modulation)

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L}\mu_{\text{eff}} C_{ox}\left(V_{GS} - V_{th}\right). \tag{1.18}$$

This can also be written as

$$g_m = \sqrt{\frac{W}{L} 2\mu_{\text{eff}} C_{ox} I_{DS}}. \tag{1.19}$$

Generally the gate length L is fixed at the minimum supported by a particular process, as this provides the highest frequency of operation. However, both L and W can be selected to control the current, I_{DS}. For example, if V_{GS} is fixed, then the MOSFET acts as a current source, with the value of the current adjusted in design by setting L and W provided that there is sufficient V_{DS}.

The current-voltage characteristics shown in Figure 1-5(d) are those of an enhancement-mode MOSFET, which requires the simplest processing. Applying a gate-source voltage enhances the channel and increases I_{DS}. With additional processing [5, 6, 10, 13] a depletion-mode MOSFET can be fabricated so that the channel exists even without an applied gate voltage. The same equations are used to describe operation with the threshold voltage changed. I_{DS} increases as the gate-source voltage increases, and it reduces as the gate-voltage becomes negative. The contrast between enhancement-mode and depletion-mode MOSFETs is illustrated in Figure 1-4.

The voltage of the bulk semiconductor affects the operation of a MOSFET and is a fourth terminal controlling drain-source conduction, but has a much smaller effect than the gate does. Most often the bulk is connected electrically to the most negative voltage in a circuit for an nMOSFET and to the most positive voltage for a pMOSFET. The standard schematic symbols of MOSFETs are shown in Table 1-2.

1.3.3 MESFET, HEMT, and JFET Fundamentals

The MESFETand HEMT are types of JFETs fabricated using compound semiconductors, with JFET most commonly referring to silicon devices only. The cross section of a JFET is shown in Figure 1-6(a), where the depth (cross section) of the conducting channel is varied by the thickness of the depletion region of a reverse-biased junction. With the silicon JFET, the voltage applied to the gate terminal changes the amount of reverse bias and hence the depletion region thickness. Increased reverse bias reduces the cross section of the current-carrying channel. Thus a JFET looks like a variable conductance. The controlling field of the FET is created at the reverse-biased pn junction at

Table 1-2: IEEE standard schematic symbols for MOSFET transistors [8] and symbols more commonly used in schematics [9]. The MOSFET symbols are for enhancement- and depletion-mode transistors. The letters indicate terminals: G (gate), D (drain), S (source), U (bulk). The three-terminal nMOSFET symbol is most often used when the bulk is connected to the most negative connection in the circuit, and the three-terminal pMOSFET symbol is used when the bulk is tied to V_{DD} (the most positive connection).

Transistor	IEEE symbol	Commonly used symbol (3 terminal)	Commonly used symbol (4 terminal)
FET, nMOS, depletion			
FET, pMOS, depletion			
FET, nMOS, enhancement			
FET, pMOS, enhancement			

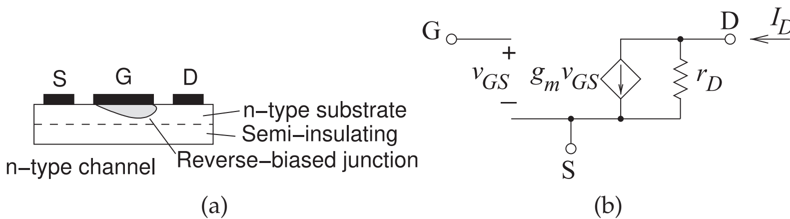
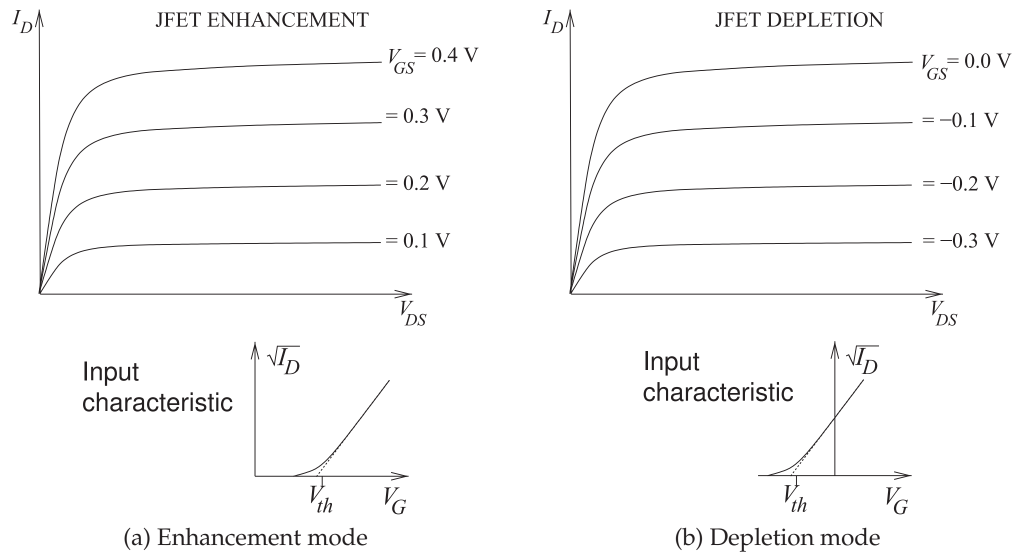


Figure 1-6: JFET details: (a) cross section; and (b) circuit model of fundamental operation.

the gate terminal. The term JFET most commonly refers to a silicon junction FET. With compound semiconductors such as GaAs, the pn junction of a silicon JFET is replaced by a Schottky barrier junction and the transistor is called a **metal-epitaxy-semiconductor FET** (**MESFET**). A device similar to the MESFET is the **high electron mobility transistor** (**HEMT**), where the field is established at the junction of two compound semiconductor materials having different band gaps, called a heterojunction. The channel is formed at the heterojunction. The HEMT is also called the **heterostructure FET** (**HFET**). A MESFET with a graded junction is called a **modulation-doped FET** (**MODFET**). A **pseudomorphic HEMT** (**pHEMT**) has an extremely thin layer establishing the channel so that the crystal structure stretches and a very high bandgap is established. Enhancement-mode and depletion-mode JFETs are contrasted in Figure 1-7.

The Materka-Kacprzak transistor model was developed for GaAs MESFET transistors [14] but is used to model silicon JFET and HEMT transistors as well. The model is described in Section 1.A.2 and the fundamental operation is described by Equation (1.64), which is repeated here without the area



(a) Enhancement mode (b) Depletion mode

Figure 1-7: Current-voltage characteristics of depletion-mode and enhancement-mode JFETs.

multiplier:

$$I_{DS} = I_{DSS}\left[1 + S_S\frac{V_{DS}}{I_{DSS}}\right]\left[1 - \frac{V_{GS}(t-\tau)}{V_{P0} + \gamma V_{DS}}\right]^{(E + K_E V_{GS}(t-\tau))} \times \tanh\left[\frac{S_L V_{DS}}{I_{DSS}(1 - K_G V_{GS}(t-\tau))}\right]. \quad (1.20)$$

Here I_{DSS} is the drain saturation current, and this, along with all quantities in Equation (1.20) other than V_{DS}, V_{GS}, and I_{DS} are constants and specified as inputs by the user. Equation (1.20) indicates that the fundamental operation of a JFET is that of a voltage-controlled current source. Thus the small-signal circuit model of fundamental operation is as shown in Figure 1-6(b).

The schematic symbols used for the MESFET, HEMT, and JFET are shown in Table 1-3. The only MESFET type used, however, is the n-type, as the p-type MESFET has poor performance due to the low mobility of holes.

Table 1-3: IEEE standard schematic symbols for JFETs (MESFET, HEMT, JFET) [8] and symbols more commonly used in schematics. The letters indicate terminals: G (gate), D (drain), S (source).

Transistor	IEEE symbol	Commonly used symbol
FET, pJFET	G D S	G D S
FET, nJFET, MESFET, HEMT	G D S	G D S

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Appendix

1.A Active Device Models

1.A.1 Level 3 MOSFET Model 14
1.A.2 Materka–Kacprzak MESFET and HEMT Model 19
1.A.3 Gummel–Poon: Bipolar Junction Transistor Model 20

This appendix presents the model parameters of the three most common transistor types used in microwave designs. These models are available in nearly all circuit simulators. Transistor models implement device equations that have been developed from physical insight with necessary simplifications required for implementation in a simulator. The purpose of presenting these models is so that the basic physical description of operation can be examined.

1.A.1 Level 3 MOSFET Model

The level 3 MOSFET model is the model of a silicon MOSFET transistor and is one of a large number of different MOSFET models that are used [15–18]. MOSFETs are the most complicated transistor to model, as their operation relies on attracting carriers into the channel under the gate in a process called inversion. The MOS level 3 model here uses the charge-conserving Yang–Chatterjee model [19] for modeling charge and capacitance. For many years the level 3 MOSFET model was implemented in circuit simulators but did not conserve charge. An example of errors that can exist in device models.

The model parameters listed in Table 1-4 can be specified by the circuit designer.

Table 1-4: Level 3 MOSFET model parameters.

Name	Description	Units	Default
gamma	Bulk threshold parameter	$V^{0.5}$	0

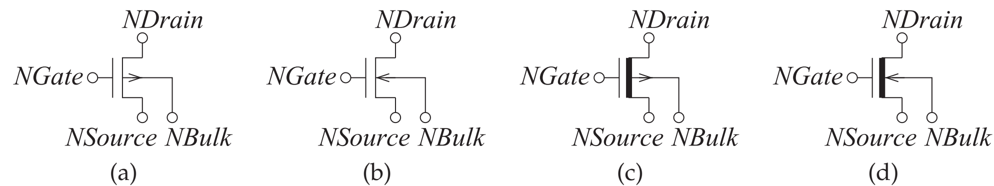


Figure 1-8: MOSFET types: (a) enhancement-mode p type; (b) enhancement-mode p type; (c) depletion-mode n type; (d) depletion-mode n type;

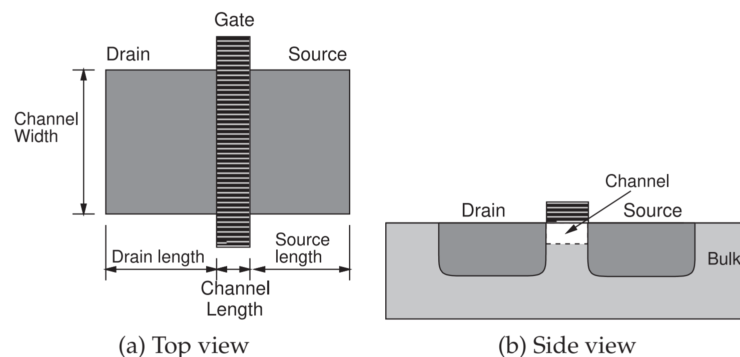


Figure 1-9: Physical layout of a MOSFET transistor.

Name	Description	Units	Default
kp	Transconductance parameter	A/V^2	0.000021
l	Device length	m	0.000002
w	Device width	m	0.00005
ld	Lateral diffusion length	m	0
wd	Lateral diffusion width	m	0
nsub	Substrate doping	cm^{-3}	0
phi	Surface inversion potential	V	0.6
tox	Oxide thickness	m	1×10^{-7}
u0	Surface mobility	$cm^2/V\text{-}s$	600
vt0	Zero bias threshold voltage	V	0
kappa	Saturation field factor	m	0.2
t	Device temperature	degrees	300.15
tnom	Nominal temperature	degrees	300.15
nfs	Fast surface state density	cm^{-2}	0
eta	Static feedback on threshold voltage		0
theta	Mobility modulation	1/V	0
tpg	Gate material type		0
nss	Surface state density	cm^{-2}	0
vmax	Maximum carrier drift velocity	m/sec	0
xj	Metallurgical junction depth		0
delta	Width effect on threshold voltage		0

Device Equations

The device equations here are specifically for a p-type MOSFET. There are sign changes required to get the appropriate current directions for an n-type MOSFET. The subscript D refers to the drain, S refers to the source, and G refers to the gate. The constants used are

$$q = 1.6021918 \times 10^{-19} \text{ (As)}, \quad k = 1.3806226 \times 10^{-23} \text{ (J/K)},$$
$$\epsilon_0 = 8.85421487 \times 10^{-12} \text{ (F/m)}, \quad \epsilon_s = 11.7\,\epsilon_0.$$

All parameters used are indicated in THIS font.

$$E_g = 1.16 - \frac{7.02 \times 10^{-4}\,\mathtt{T}^2}{\mathtt{T} + 1108} \text{ (V)} \qquad C_{ox} = \frac{\epsilon_0\,3.9}{\mathtt{TOX}} \text{ (F)} \tag{1.21}$$

$$L_{\text{eff}} = \mathtt{L} - 2\,\mathtt{LD} \qquad W_{\text{eff}} = \mathtt{W} - 2\,\mathtt{WD} \tag{1.22}$$

Depletion layer width coefficient:

$$X_d = \sqrt{\frac{2\,\epsilon_s}{q\,\mathtt{NSUB}\,10^6}}. \tag{1.23}$$

Built in voltage:

$$V_{bi} = \mathtt{VT0} - \mathtt{GAMMA}\sqrt{\mathtt{PHI}}. \tag{1.24}$$

Square root of substrate voltage:

$$\begin{aligned} V_{BS} \le 0 &\implies SqV_{BS} = \sqrt{\mathtt{PHI} - V_{BS}} \\ V_{BS} > 0 &\implies SqV_{BS} = \sqrt{\frac{\mathtt{PHI}}{1 + \frac{0.5}{\mathtt{PHI}} V_{BS}(1 + \frac{0.75}{\mathtt{PHI}} V_{BS})}}. \end{aligned} \tag{1.25}$$

Short-channel effect correction factor:
In a short-channel device, the device threshold voltage tends to be lower since part of the depletion charge in the bulk terminates the electric fields at the source and drain. The value of this correction factor is determined by the metallurgical depth, XJ.

$$c_0 = 0.0631353 \tag{1.26}$$
$$c_1 = 0.8013292 \tag{1.27}$$
$$c_2 = -0.01110777 \tag{1.28}$$
$$T_1 = \mathtt{XJ}\,(c_0 + c_1\, X_d\, SqV_{BS} + c_2\,(X_d\, SqV_{BS})^2) \tag{1.29}$$
$$F_s = 1 - \frac{\mathtt{LD} + T_1}{L_{\text{eff}}}\sqrt{1 - \left(\frac{X_d\, SqV_{BS}}{\mathtt{XJ} + X_d\, SqV_{BS}}\right)^2}. \tag{1.30}$$

Narrow-channel effect correlation factor:
The edge effects in a narrow channel cause the depletion charge to extend beyond the width of the channel. This has the effect of increasing the threshold voltage:

$$F_n = \frac{\pi\, \epsilon_s\, \mathtt{DELTA}}{2\, C_{ox}\, W_{\text{eff}}}. \tag{1.31}$$

Static feedback coefficient:
The threshold voltage lowers because the charge under the gate terminal depleted by the drain junction field increases with V_{DS}. This effect is drain-induced barrier lowering (DIBL):

$$\sigma = \frac{8.14 \times 10^{-22}\, \mathtt{ETA}}{{L_{\text{eff}}}^3\, C_{ox}}. \tag{1.32}$$

Threshold voltage:

$$V_{th} = V_{bi} - \sigma\, V_{DS} + \mathtt{GAMMA}\, SqV_{BS}\, F_s\, + F_n\, SqV_{BS}{}^2. \tag{1.33}$$

Subthreshold operation:
This variable is invoked depending on the value of the parameter NFS and is used only when in the subthreshold mode:

$$X_n = 1 + \frac{q\,\mathtt{NFS}\,10^4}{C_{ox}} + \frac{F_n}{2} + \frac{\mathtt{GAMMA}}{2}\,\frac{F_s}{SqV_{BS}}. \tag{1.34}$$

Modified threshold voltage:
This variable defines the limit between weak and strong inversion:

$$\begin{array}{lll} \mathtt{NFS} > 0 & \Longrightarrow & V_{on} = V_{th} + \frac{kT}{q}\, X_n \\ \mathtt{NFS} \leq 0 & \Longrightarrow & V_{on} = V_{th}. \end{array} \tag{1.35}$$

Subthreshold gate voltage:

$$V_{gsx} = \text{MAX}(V_{GS}, V_{on}). \tag{1.36}$$

Surface mobility:

$$\mu_s = \frac{\mathtt{U0}10^{-4}}{1 + \mathtt{THETA}(V_{gsx} - V_{th})}. \tag{1.37}$$

Saturation voltage:
Calculation of this voltage requires many steps. The effective mobility is calculated as

$$\mu_{\text{eff}} = \mu_s\, F_{\text{drain}}, \tag{1.38}$$

where

$$F_{\text{drain}} = \left(1 + \frac{\mu_s\, V_{DS}}{\texttt{VMAX}\, L_{\text{eff}}}\right)^{-1} \tag{1.39}$$

$$\beta = \frac{W_{\text{eff}}}{L_{\text{eff}}}\, \mu_{\text{eff}}\, C_{ox}. \tag{1.40}$$

The Taylor expansion of bulk charge is

$$F_B = \frac{\texttt{GAMMA}}{4}\, \frac{F_s}{SqV_{BS}} + 2\, F_n. \tag{1.41}$$

The standard value of the saturation voltage is calculated as

$$V_{\text{sat}} = \frac{V_{gsx} - V_{th}}{1 + F_B}. \tag{1.42}$$

The final value of the saturation voltage depends on the parameter `VMAX`:

$$\begin{array}{lll} \texttt{VMAX} = 0 & \Longrightarrow & V_{\text{dsat}} = V_{\text{sat}} \\ \texttt{VMAX} > 0 & \Longrightarrow & V_{\text{dsat}} = V_{\text{sat}} + V_c - \sqrt{V_{\text{sat}}^2 + V_c^2}, \quad V_c = \texttt{VMAX}\, L_{\text{eff}}/\mu_s. \end{array} \tag{1.43}$$

Velocity saturation drain voltage:
This ensures that the drain voltage does not exceed the saturation voltage:

$$V_{dsx} = \text{MIN}(V_{DS}, V_{\text{dsat}}). \tag{1.44}$$

Drain current:
Linear region:

$$I_{DS} = \beta\, \frac{\mu_s}{\texttt{U0}\; 10^{-4}}\, F_{\text{drain}}\, (V_{gsx} - V_{th} - \frac{1 + F_B}{2}\, V_{dsx})\, V_{dsx}. \tag{1.45}$$

Saturation region:

$$I_{DS} = \beta\, \left[(V_{GS} - V_{th}) - \frac{1 + F_B}{2}\, V_{\text{dsat}}\right] V_{\text{dsat}}. \tag{1.46}$$

Using Equation (1.40), this becomes

$$I_{DS} = \frac{W_{\text{eff}}}{L_{\text{eff}}}\, \mu_{\text{eff}}\, C_{ox}\, \left[(V_{GS} - V_{th}) - \frac{1 + F_B}{2}\, V_{\text{dsat}}\right] V_{\text{dsat}}. \tag{1.47}$$

Cutoff region:

$$I_{DS} = 0. \tag{1.48}$$

Channel length modulation:
As V_{DS} increases beyond V_{dsat}, the point where the carrier velocity begins to saturate moves toward the source. This is modeled by the term $\triangle_\ell$:

$$\triangle_\ell = X_d\, \sqrt{\frac{X_d^2\, E_p^2}{4} + \texttt{KAPPA}\, (V_{DS} - V_{\text{dsat}})} - \frac{E_p\, X_d^2}{2}, \tag{1.49}$$

where E_p is the lateral field at pinch-off and is given by

$$E_p = \frac{\texttt{VMAX}}{\mu_s\,(1 - F_{\text{drain}})} \tag{1.50}$$

The drain current is multiplied by a correction factor, l_{fact}. This factor prevents the denominator $(L_{\text{eff}} - \triangle_\ell)$ from going to zero:

$$\begin{array}{lll} \triangle_\ell \le 0.5\,L_{\text{eff}} & \Longrightarrow & l_{\text{fact}} = \frac{L_{\text{eff}}}{L_{\text{eff}} - \triangle_\ell} \\ \triangle_\ell > 0.5\,L_{\text{eff}} & \Longrightarrow & l_{\text{fact}} = \frac{4\,\triangle_\ell}{L_{\text{eff}}}. \end{array} \tag{1.51}$$

The corrected value of the drain-source current is

$$I_{DS\text{new}} = I_{DS}\,l_{\text{fact}}. \tag{1.52}$$

Subthreshold operation:
For subthreshold operation, if the fast surface density parameter NFS is specified and $V_{GS} \le V_{\text{on}}$, then the final value of the drain-source current is given by

$$I_{DS\text{final}} = I_{DSnew}\,\mathrm{e}^{\frac{kt}{q}\,\frac{V_{GS} - V_{\text{on}}}{X_n}}. \tag{1.53}$$

Yang–Chatterjee charge model [19]
This model ensures continuity of the charges and capacitances throughout different regions of operation. The intermediate quantities are

$$V_{FB} = V_{to} - \texttt{GAMMA}\,\sqrt{\texttt{PHI}} - \texttt{PHI} \tag{1.54}$$

and

$$C_o = C_{ox}\,W_{\text{eff}}\,L_{\text{eff}}. \tag{1.55}$$

Accumulation region, $V_{GS} \le V_{FB} + V_{BS}$:

$$Q_d = 0, \quad Q_s = 0, \quad Q_b = -C_o\,(V_{GS} - V_{FB} - V_{BS}). \tag{1.56}$$

Cutoff region, $V_{FB} + V_{BS} < V_{GS} \le V_{th}$:

$$Q_d = 0, \quad Q_s = 0, \quad Q_b = -C_o\,\frac{\texttt{GAMMA}^2}{2}\,\{-1 + \sqrt{1 + \frac{4\,(V_{GS} - V_{FB} - V_{BS})}{\texttt{GAMMA}^2}}\}. \tag{1.57}$$

Saturation region, $V_{th} < V_{GS} \le V_{DS} + V_{th}$:

$$Q_d = 0, \quad Q_s = -\tfrac{2}{3}\,C_o\,(V_{GS} - V_{th}), \quad Q_b = C_o\,(V_{FB}\,\texttt{PHI} - V_{th}). \tag{1.58}$$

Linear region, $V_{GS} > V_{DS} + V_{th}$:

$$Q_d = -C_o\,\left[\frac{V_{DS}^2}{8\,(V_{GS} - V_{th} - \frac{1}{2}V_{DS})} + \frac{V_{GS} - V_{th}}{2} - \frac{3}{4}\,V_{DS}\right] \tag{1.59}$$

$$Q_s = -C_o\,\left[\frac{V_{DS}^2}{24\,(V_{GS} - V_{th} - \frac{1}{2}V_{DS})} + \frac{V_{GS} - V_{th}}{2} + \frac{1}{4}\,V_{DS}\right] \tag{1.60}$$

$$Q_b = C_o\,(V_{FB}\,\texttt{PHI} - V_{th}). \tag{1.61}$$

The final currents at the transistor nodes are given by

$$I_d = I_{DS\text{final}} + \frac{dQ_d}{dt} \qquad I_g = \frac{dQ_g}{dt} \qquad I_s = -I_{DS\text{final}} + \frac{dQ_s}{dt}. \tag{1.62}$$

1.A.2 Materka–Kacprzak MESFET Model

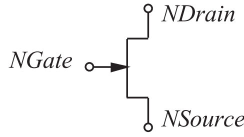


Figure 1-10: MESFET element.

The Materka–Kacprzak transistor model was developed for GaAs MESFET transistors [14] but is used to model silicon JFETs and compound semiconductor HEMT transistors as well. It is based on physical interpretation of a transistor with a junction-based gate. There are a number of other models [20–22], but the Materka–Kacprzak model is representative of JFETs.

Table 1-5: Materka–Kacprzak model parameters

Name	Description	Units	Default
AFAB	Slope factor of breakdown current ($AFAB$)	$1/V$	0.0
AFAG	Slope factor of gate conduction current ($AFAG$)	$1/V$	38.696
AREA	Area multiplier ($AREA$)	-	1.0
C10	Gate source Schottky barrier capacitance for (C_{10})	F	0.0
CFO	Gate drain feedback capacitance for (C_{F0})	F	0.0
CLS	Constant parasitic component of gate-source capacitance (C_{LS})	F	0.0
E	Constant part of power law parameter (E)	-	2.0
GAMA	Voltage slope parameter of pinch-off voltage (γ)	$1/V$	0.0
IDSS	Drain saturation current for (I_{DSS})	A	0.1
IG0	Saturation current of gate-source Schottky barrier (I_{G0})	A	0.0
K1	Slope parameter of gate-source capacitance (K_1)	$1/V$	1.25
KE	Dependence of power law on V_{GS} , (K_E)	$1/V$	0.0
KF	Slope parameter of gate-drain feedback capacitance (K_F)	$1/V$	1.25
KG	Drain dependence on V_{GS} in the linear region, (K_G)	$1/V$	0.0
KR	Slope factor of intrinsic channel resistance (K_R)	$1/V$	0.0
RI	Intrinsic channel resistance for (R_I)	Ω	0.0
SL	Slope of the drain characteristic in the saturated region, (S_L)	S	0.15
SS	Slope of the drain characteristic in the saturated region (S_S)	S	0.0
T	Channel transit-time delay (τ)	s	0.0
VBC	Breakdown voltage (V_{BC})	V	10^{10}
VP0	Pinch-off voltage for (V_{P0})	V	-2.0

The physical constants used in the model evaluation are

k	the Boltzmann constant	$1.3806226\,10^{-23}$ J/K
q	electronic charge	$1.6021918\,10^{-19}$ C

Standard calculations:

$$V_{\mathrm{TH}} = (kT)/q, \tag{1.63}$$

where T is the analysis temperature. Also

V_{DS} is the intrinsic drain source voltage,
V_{GS} is the intrinsic gate source voltage, and
V_{GD} is the intrinsic gate drain voltage.

Device Equations

Current characteristics:

$$I_{DS} = \text{Area} I_{DSS} \left[1 + S_S \frac{V_{DS}}{I_{DSS}}\right] \left[1 - \frac{V_{GS}(t-\tau)}{V_{P0} + \gamma V_{DS}}\right]^{(E + K_E V_{GS}(t-\tau))} \times \tanh\left[\frac{S_L V_{DS}}{I_{DSS}(1 - K_G V_{GS}(t-\tau))}\right] \quad (1.64)$$

$$I_{GS} = \text{Area} I_{G0} \left[\mathrm{e}^{A_{FAG} V_{GS}} - 1\right] - I_{B0} \left[e^{-A_{FAB}(V_{GS} + V_{BC})}\right] \quad (1.65)$$

$$I_{GD} = \text{Area} I_{G0} \left[\mathrm{e}^{A_{FAG} V_{GD}} - 1\right] - I_{B0} \left[e^{-A_{FAB}(V_{GD} + V_{BC})}\right] \quad (1.66)$$

$$R_I = \begin{cases} R_{10}(1 - K_R V_{GS})/\text{Area} & K_R V_{GS} < 1.0 \\ 0 & K_R V_{GS} \geq 1.0\,. \end{cases} \quad (1.67)$$

Capacitance:

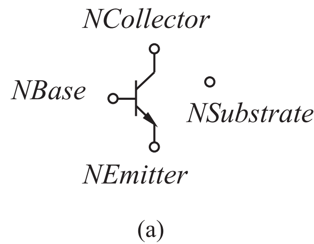
C_{LVL} = 1 (default) for the standard Materka–Kacprzak capacitance model described below is used. The Materka–Kacprzak capacitances are

$$C'_{DS} = C_{DS} \quad (1.68)$$

$$C'_{GS} = \begin{cases} \left[C_{10}(1 - K_1 V_{GS})^{M_{GS}} + C_{1S}\right] & K_1 V_{GS} < F_{CC} \\ \left[C_{10}(1 - F_{CC})^{M_{GS}} + C_{1S}\right] & K_1 V_{GS} \geq F_{CC} \end{cases} \quad (1.69)$$

$$C'_{GD} = \begin{cases} \text{Area}\left[C_{F0}(1 - K_1 V_1)^{M_{GD}}\right] & K_1 V_1 < F_{CC} \\ \text{Area}\left[C_{F0}(1 - F_{CC})^{M_{GD}}\right] & K_1 V_1 \geq F_{CC} \end{cases}\,. \quad (1.70)$$

1.A.3 Gummel–Poon: Bipolar Junction Transistor Model



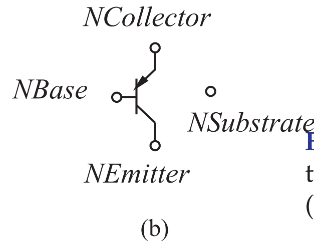


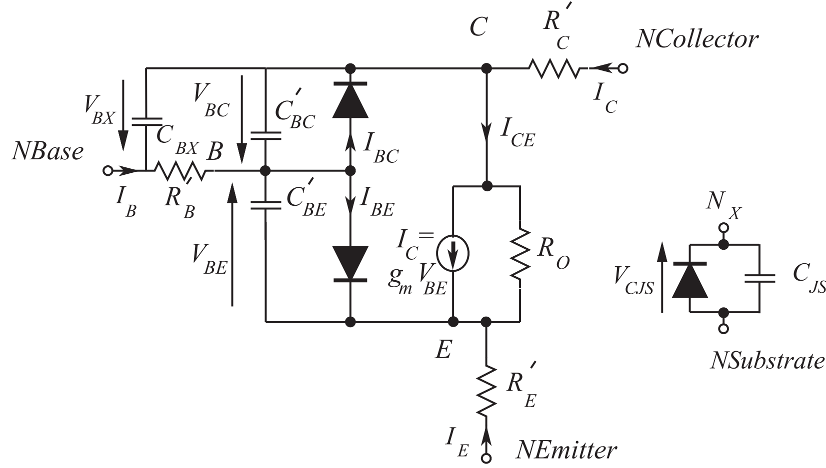
Figure 1-11: Q — bipolar junction transistor: (a) npn transistor; (b) pnp transistor.

Bipolar transistor models are based on the Gummel–Poon model [7] described here. The key feature of the model is that it captures the dependence of the forward and reverse current gain on current. In essence, the BJT model is a current-controlled current source. The Gummel–Poon model and its derivatives are used to model silicon BJTs and compound semiconductor HBTs [23, 24].

Table 1-6: Gummel–Poon BJT model parameters

Name	Description	Units	Default
AREA	Current multiplier		1.0
BF	Ideal maximum forward beta (B_F)		100.0
BR	Ideal maximum reverse beta (B_R)		1.0
C2	Base-emitter leakage saturation coefficient		I_{SE}/I_S
C4	Base-collector leakage saturation coefficient		(I_{SC}/I_S)
CJC	Base collector zero bias p-n capacitance (C_{JC})	F	0.0

Name	Description	Units	Default
CJE	Base emitter zero bias p-n capacitance (C_{JE})	F	0.0
EG	Bandgap voltage (E_G)	eV	1.11
FC	Forward bias depletion capacitor coefficient (F_C)		0.5
IKF	Corner of forward beta high-current roll-off (I_{KF})	A	10^{-10}
IKR	Corner for reverse-beta high current roll off (I_{KR})		10^{-10}
IS	Transport saturation current (I_S)	A	10^{-16}
ISC	Base collector leakage saturation current (I_{SC})	A	0.0
ISE	Base-emitter leakage saturation current (I_{SE})	A	0.0
IRB	Current at which RB falls to half of R_{BM} (I_{RB})	A	10^{-10}
ITF	Transit time dependency on IC (I_{TF})	A	0.0
MJC	Base collector p-n grading factor (M_{JC})		0.33
MJE	Base emitter p-n grading factor (M_{JE})		0.33
NC	Base-collector leakage emission coefficient (N_C)		2.0
NE	Base-emitter leakage emission coefficient (N_E)		1.5
NF	Forward current emission coefficient (N_F)		1.0
NR	Reverse current emission coefficient (N_R)		1.0
RB	Zero bias base resistance (R_B)	Ω	0.0
RBM	Minimum base resistance (R_{BM})	Ω	R_B
RE	Emitter ohmic resistance (R_E)	Ω	0.0
RC	Collector ohmic resistance (R_C)	Ω	0.0
T	Operating Temperature T	K	300
TF	Ideal forward transit time (T_S)	secs	0.0
TNOM	Nominal temperature (T_{NOM})	K	300
TR	Ideal reverse transit time (T_R)	S	0.0
TRB1	RB temperature coefficient (linear) (T_{RB1})		0.0
TRB2	RB temperature coefficient (quadratic) (T_{RB2})		0.0
TRC1	RC temperature coefficient (linear) (T_{RC1})		0.0
TRC2	RC temperature coefficient (linear) (T_{RC2})		0.0
TRE1	RE temperature coefficient (linear) (T_{RE1})		0.0
TRE2	RE temperature coefficient (quadratic) (T_{RE2})		0.0
TRM1	RBM temperature coefficient (linear) (T_{RM1})		0.0
TRM2	RBM temperature coefficient (quadratic) (T_{RM2})		0.0
VA	Alternative keyword for VAF (V_A)	V	10^{-10}
VAF	Forward early voltage (V_{AF})	V	10^{-10}
VAR	Reverse early voltage (V_{AR})		10^{-10}
VB	alternative keyword for VAR (V_B)		10^{-10}
VJC	Base collector built in potential (V_{JC})	V	0.75
VJE	Base emitter built in potential (V_{JE})	V	0.75
VTF	Transit time dependency on VBC (V_{TF})	V	10^{-10}
XCJC	Fraction of CBC connected internal to RB (X_{CJC})		1.0
XTB	Forward and reverse beta temperature coefficient (X_{TB})		0.0
XTF	Transit time bias dependence coefficient (X_{TF})		0.0
XTI	IS temperature effect exponent (X_{TI})		3.0



BJT model schematic.

Standard Calculations

The physical constants used in the model evaluation are

k	the Boltzmann constant	$1.3806226\,10^{-23}$ J/K
q	electronic charge	$1.6021918\,10^{-19}$ C

Absolute temperatures (in kelvin, K) are used. The thermal voltage is

$$V_{\mathrm{TH}}(T_{\mathrm{NOM}}) = k\,T_{\mathrm{NOM}}/q. \tag{1.71}$$

Current characteristics:
The base-emitter current is

$$I_{BE} = I_{BF}/\beta_F + I_{LE}. \tag{1.72}$$

the base-collector current is

$$I_{BC} = I_{BR}/\beta_R + I_{LC}. \tag{1.73}$$

The collector-emitter current is

$$I_{CE} = I_{BF} - I_{BR}/K_{QB}, \tag{1.74}$$

where the forward diffusion current is

$$I_{BF} = I_S\left(\mathrm{e}^{V_{BE}/(N_F V_{\mathrm{TH}})} - 1\right). \tag{1.75}$$

The nonideal base-emitter current is

$$I_{LE} = I_{SE}\left(\mathrm{e}^{V_{BE}/(N_E V_{\mathrm{TH}})} - 1\right). \tag{1.76}$$

The reverse diffusion current is

$$I_{BR} = I_S\left(\mathrm{e}^{V_{BC}/(N_R V_{\mathrm{TH}})} - 1\right). \tag{1.77}$$

The nonideal base-collector current is

$$I_{LC} = I_{SC}\left(\mathrm{e}^{V_{BC}/(N_C V_{\mathrm{TH}})} - 1\right). \tag{1.78}$$

The base charge factor is

$$K_{QB} = 1/2\left[1 - V_{BC}/V_{AF} - V_{BE}/V_{AB}\right]^{-1}\left(1 + \sqrt{1 + 4\left(I_{BF}/I_{KF} + I_{BR}/I_{KR}\right)}\right). \quad (1.79)$$

Thus the conductive current flowing into the base is

$$I_B = I_{BE} + I_{BC}, \quad (1.80)$$

the conductive current flowing into the collector is

$$I_C = I_{CE} - I_{BC}, \quad (1.81)$$

and the conductive current flowing into the emitter is

$$I_E = I_{BE} + I_{CE}. \quad (1.82)$$

Capacitances

$C_{BE} = \text{Area}(C_{BE\tau} + C_{BEJ})$, where the base-emitter transit time or diffusion capacitance is

$$C_{BE\tau} = \tau_{F,\text{EFF}}\left(\partial I_{BF}/\partial V_{BE}\right) \quad (1.83)$$

and the effective base transit time is empirically modified to account for base punchout, space-charge limited current flow, quasi-saturation, and lateral spreading, which tend to increase τ_F:

$$\tau_{F,\text{EFF}} = \tau_F\left[1 + X_{TF}(3x^2 - 2x^3)\text{e}^{\left(V_{BC}/(1.44V_{TF})\right)}\right], \quad (1.84)$$

and $x = I_{BF}/(I_{BF} + \text{Area}I_{TF})$.

The base-emitter junction (depletion) capacitance is

$$C_{BEJ} = \begin{cases} C_{JE}\left(1 - V_{BE}/V_{JE}\right)^{-M_{JE}} & V_{BE} \le F_C V_{JE} \\ C_{JE}\left(1 - F_C\right)^{-(1 + M_{JE})}\left(1 - F_C(1 + M_{JE}) + M_{JE}V_{BE}/V_{JE}\right) & V_{BE} > F_C V_{JE}. \end{cases} \quad (1.85)$$

The base-collector capacitance is $C_{BC} = \text{Area}(C_{BC\tau} + X_{CJC}C_{BCJ})$, where the base-collector transit time or diffusion capacitance is

$$C_{BC\tau} = \tau_R \partial I_{BR}/\partial V_{BC}. \quad (1.86)$$

The base-collector junction (depletion) capacitance is

$$C_{BCJ} = \begin{cases} C_{JC}\left(1 - V_{BC}/V_{JC}\right)^{-M_{JC}} & V_{BC} \le F_C V_{JC} \\ C_{JC}\left(1 - F_C\right)^{-(1 + M_{JC})}\left(1 - F_C(1 + M_{JC}) + M_{JC}V_{BC}/V_{JC}\right) & V_{BC} > F_C V_{JC}. \end{cases} \quad (1.87)$$

The capacitance between the extrinsic base and the intrinsic collector is

$$C_{BX} = \begin{cases} \text{Area}(1 - X_{CJC})C_{JC}\left(1 - V_{BX}/V_{JC}\right)^{-M_{JC}} & V_{BX} \le F_C V_{JC} \\ (1 - X_{CJC})C_{JC}\left(1 - F_C\right)^{-(1 + M_{JC})} & V_{BX} > F_C V_{JC} \\ \quad \times\ \left(1 - F_C(1 + M_{JC}) + M_{JC}V_{BX}/V_{JC}\right) & \end{cases}. \quad (1.88)$$

The substrate junction capacitance is

$$C_{JS} = \begin{cases} \text{Area}C_{JS}\left(1 - V_{CJS}/V_{JS}\right)^{-M_{JS}} & V_{CJS} \le 0 \\ \text{Area}C_{JS}\left(1 + M_{JS}V_{CJS}/V_{JS}\right) & V_{CJS} > 0. \end{cases} \quad (1.89)$$

CHAPTER 2

Linear Amplifiers

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2.1 Introduction

Amplifiers increase the power of an RF signal by converting DC power to AC power. Amplifiers can be optimized for low noise, moderate to high gain, high efficiency, low distortion, or specific output power. At the same time stability must be assured, which is a problem with feedback due to parasitics and the internal feedback of transistors. However, it is not possible to optimize all of the parameters simultaneously. This has led to several amplifier design strategies and amplifier topologies trading off design complexity and performance. In this chapter the major active devices and linear amplifiers based on them are examined. A critical common aspect is minimizing noise, maximizing the efficiency of power conversion to RF, and ensuring stability.

A common characteristic of linear amplifier design, the subject of this chapter, is that the operation of the amplifier at RF is similar to its operation at low frequencies. The design strategy is based on small signal design and it is sufficient to use the small-signal S parameters of a device at the chosen operating point. In contrast, the design of power amplifiers considered in a future chapter is more complicated, as the amplifier operation is dependent on the signal level and design must use the large signal model of transistors and use nonlinear simulators.

2.2 Linear Amplifier Design Strategies

Linear amplifier design requires that the transistor(s) be biased in a high-gain region and that input and output matching networks be used to provide good power transfer at the input and output of the transistor stages. This circuit arrangement is shown in Figure 2-1. The DC bias control circuit is fairly standard; it does not involve any microwave constraints. The lowpass filters (in the bias circuits) can have one of several forms and are often integrated into the input and output matching networks. Synthesis of the input and output matching networks (and occasionally a feedback network required for stability and broadband operation) is the primary objective of any amplifier design.

RF transistors used to amplify small signals should have high maximum available gain and low noise characteristics. For transistors used in transmitters, where the efficient generation of power is critical, it is important to linear amplifier design that the transistor characteristics be close to linear in the central region of the output current-voltage characteristics so that distortion is minimized. The ultimate limit on output power is determined by the breakdown voltage at high drain-source voltages and also by the maximum current density that can be supported. Finally, for efficient amplification of large signals, the knee voltage (where the current-voltage curves bend over and starts to flatten) should be low.

Manufacturers of discrete transistors and amplifier modules provide substantial information, including S parameters and, in some cases, reference designs. An extract from the datasheet of a pHEMT transistor is shown in Figure 2-2. The intended application is provided and the device structure has been optimized for the application.

Design examples presented in the next few sections will use the pHEMT transistor documented in Figure 2-2. This discrete transistor is described as a low-noise, high-frequency, packaged pHEMT that can be used in amplifiers operating at up to 18 GHz. It shares a common characteristic of FET devices in that S_{21} is highest at low frequencies and the feedback parameter, S_{12}, is lowest at low frequencies. This means that gain is harder to achieve at higher frequencies and the higher-level feedback means that stability is often a problem at higher frequencies. However, the loop gain described by $S_{21}S_{12}$ is large at low frequencies so stability is also a problem at low frequencies.

2.3 Amplifier Gain Definitions

As with all circuit design, a few figures of merit (FOMs) are used to guide design. The most important metric in amplifier design is the gain

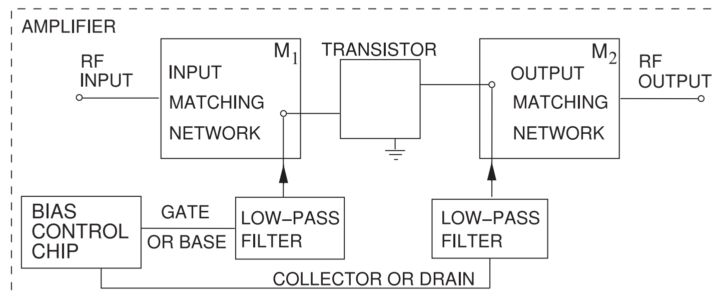


Figure 2-1: Block diagram of an RF amplifier including biasing networks.

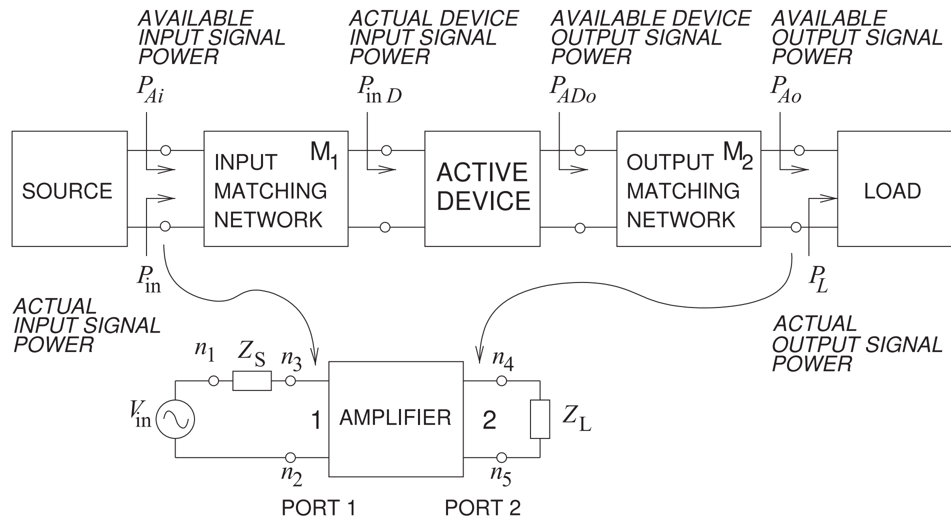
Data Sheet Extract.

Transistor technology:	Depletion-mode pHEMT.
Model:	FPD6836P70 from QORVO, Inc.
Description:	Low-noise, high-frequency packaged pHEMT.
	Optimized for low-noise, high-frequency applications.
Synopsis:	22 dBm output power (P1dB).
	15 dB power gain (G1dB) at 5.8 GHz, Usable gain to 18 GHz.
	0.8 dB noise figure at 5.8 GHz, 32 dBm output IP3 at 5.8 GHz.
	45% power-added efficiency at 5.8 GHz.
	Usable gain to 18 GHz.

Frequency (GHz)	$\|S_{11}\|$	$\angle S_{11}$ degrees	$\|S_{21}\|$	$\angle S_{21}$ degrees	$\|S_{12}\|$	$\angle S_{12}$ degrees	$\|S_{22}\|$	$\angle S_{22}$ degrees
0.500	0.976	−20.9	11.395	161.5	0.011	78.3	0.635	−11.5
1.000	0.925	−41.3	10.729	145.1	0.021	67.8	0.614	−22.2
2.000	0.796	−78.2	8.842	116.7	0.034	51.4	0.553	−37.9
3.000	0.694	−106.8	7.180	94.5	0.041	40.4	0.506	−48.9
4.000	0.614	−127.3	6.002	76.7	0.044	33.9	0.475	−57.7
5.000	0.555	−147.0	5.249	60.3	0.048	28.4	0.453	−66.4
6.000	0.511	−170.2	4.729	43.7	0.052	23.3	0.438	−76.0
7.000	0.493	163.9	4.261	26.8	0.057	14.0	0.391	−87.6
8.000	0.486	140.4	3.784	11.2	0.057	6.4	0.340	−99.1
9.000	0.473	122.5	3.448	−2.4	0.059	5.2	0.332	−109.6
10.000	0.488	103.4	3.339	−17.3	0.073	0.9	0.355	−124.8
11.000	0.539	79.8	3.166	−35.0	0.086	−10.1	0.349	−145.6
12.000	0.626	60.8	2.877	−51.9	0.095	−21.4	0.307	−169.6
13.000	0.685	47.6	2.604	−68.2	0.100	−32.5	0.295	165.3
14.000	0.724	36.2	2.392	−83.8	0.106	−43.3	0.312	142.7
15.000	0.787	20.9	2.225	−99.7	0.109	−55.1	0.320	125.4
16.000	0.818	5.2	2.067	−116.6	0.112	−68.4	0.340	103.9
17.000	0.831	−9.6	1.855	−134.4	0.108	−83.5	0.373	76.1
18.000	0.852	−19.5	1.603	−148.6	0.103	−94.2	0.406	54.7
19.000	0.815	−20.5	1.440	−159.3	0.102	−103.0	0.449	43.1
20.000	0.780	−26.8	1.382	−171.2	0.106	−113.5	0.460	37.9
21.000	0.779	−46.8	1.333	171.2	0.109	−130.7	0.438	31.4
22.000	0.786	−62.1	1.195	152.0	0.110	−148.4	0.417	6.0
23.000	0.774	−70.1	1.073	137.2	0.108	−162.4	0.428	−16.5
24.000	0.744	−81.7	1.025	123.5	0.112	−175.2	0.433	−29.0
25.000	0.704	−90.9	1.061	107.3	0.132	170.0	0.396	−46.5
26.000	0.677	−111.1	1.065	85.8	0.148	147.8	0.298	−71.0

Figure 2-2: Scattering parameters of an enhancement mode pHEMT transistor biased at $V_{DS} = 5$ V, $I_D = 55$ mA, $V_{GS} = -0.42$ V. Extract from the data sheet of the FPD6836P70 discrete transistor [1].

of the overall amplifier. There are a surprisingly large number of different definitions of gain that are useful at different stages in the design process. Each provides information about the performance of an amplifier and using the full set enables design to be approached in a systematic way. The FOMs are used to describe the performance of an amplifier, to develop an understanding of the active device, to compare different active devices, and,



Power	Description
P_{in}	Actual input power delivered to the amplifier.
P_{Ai}	Available input power from the source. $P_{\text{in}} \leq P_{Ai}$. If M_1 provides conjugate matching as seen from the source, then $P_{\text{in}} = P_{Ai}$.
$P_{\text{in}D}$	Actual device input power delivered to the active device. $P_{\text{in}D} \leq P_{\text{in}}$. If M_1 is lossless, $P_{\text{in}D} = P_{\text{in}}$.
P_{ADo}	Available device output power of the active device.
P_{Ao}	Available amplifier output power. $P_{Ao} \leq P_{ADo}$. If M_2 is lossless, $P_{Ao} = P_{ADo}$.
P_L	Actual output power delivered to load. Amplifier output power. $P_L \leq P_{Ao}$. If M_2 is lossless and provides conjugate matching, $P_L = P_{Ao} = P_{ADo}$.

Figure 2-3: Parameters used in defining gain measures. The input and output matching networks are lossless so that the actual device input signal power, $P_{\text{in}D}$, is the power delivered by the source. Similarly the actual output signal power delivered to the load, P_L, is the power delivered by the active device (the transistor including biasing network).

coupled with experience, to formulate an idea of how difficult a design will be.

The quantities used in the various gain definitions are defined in Figure 2-3. The power delivered to the amplifier is P_{in}, and this is equal to the available input power from the source if the source is conjugately matched to the input matching network. The power delivered to the active device, $P_{\text{in}D}$, is equal to the amplifier input power, P_{in}, if the input matching network is lossless. The available output power from the active device, P_{Ao}, is the actual device output power, P_o, delivered to the output matching network if the output of the active device is conjugately matched. This power is also delivered to the load as P_L if M_2 is lossless. In summary,

$P_{\text{in}} = P_{Ai}$, if the generator is conjugately matched
$P_{\text{in}} = P_{\text{in}D}$, if M_1 is lossless
$P_o = P_{Ao}$, if the output of active device is conjugately matched
$P_L = P_o$, if M_2 is lossless.

These power definitions refer to different circuit conditions. This enables a number of different gain definitions to be developed that relate to different stages in the development of an amplifier and indicate the ultimate performance achievable from an amplifier. The basic gain definitions are

- ***System gain***:
$$G = \frac{P_L}{P_{\textbf{in}}}. \tag{2.1}$$
The system gain is the power actually delivered to the load relative to the input power delivered by the source. This gain is sometimes called the **actual power gain**.

- ***Power gain***:
$$G_P = \frac{P_L}{P_{\text{in},D}}. \tag{2.2}$$
This gain is G, but with the loss of M_1 removed.

- ***Transducer gain***:
$$G_T = \frac{P_L}{P_{Ai}}. \tag{2.3}$$
This is the ratio of the power delivered to the load divided by the power available from the source. This is the gain that really matters, the power actually delivered to the load relative to the power available from the source.

- ***Available gain***:
$$G_A = \frac{P_{Ao}}{P_{Ai}}. \tag{2.4}$$
The transducer gain is the power available to the load relative to the input power available from the source. This gain is G_T with optimum M_2. That is, G_A is the system gain G with lossless M_1 and M_2 both optimized for maximum power transfer.

These gains are measures that can be used to characterize the performance of an amplifier but do not guide design. The development of guidelines begins by developing expressions for gains using the device's S parameters and then considering gain under idealized conditions such as optimum matching networks or with the device adjusted using feedback so that it is effectively unilateral.

EXAMPLE 2.1 Amplifier Gain

A source that drives an amplifier has an available output power of 1 mW. However, the load of the amplifier is mismatched so that the load reflection coefficient is 1 dB. The power actually delivered to the load of the amplifier is 1 W. Is it possible to determine the system gain? If so, what is it in decibels?

Solution:

There are many gain definitions so the information provided must be examined. The power delivered to the load is $P_L = 1$ W, and the available input power $P_{Ai} = 1$ mW. Examining the gains defined in Equations (2.1)–(2.4), Equation (2.3) yields

$$G_T = \frac{P_L}{P_{Ai}} = \frac{1\text{W}}{1\text{ mW}} = 1000 = 30\text{ dB}. \tag{2.5}$$

No other gain can be determined, i.e., the system gain cannot be determined as the actual input power is unknown.

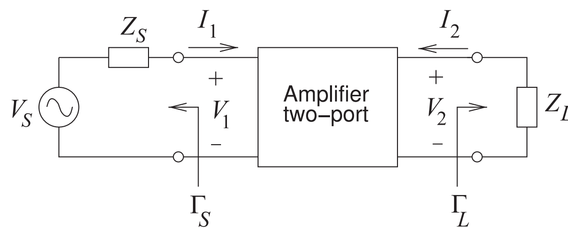
2.3.1 Gain in Terms of Scattering Parameters

This section develops the generalized scattering parameters of an amplifier and leads to expressions for gain in terms of the S parameters of the active device.

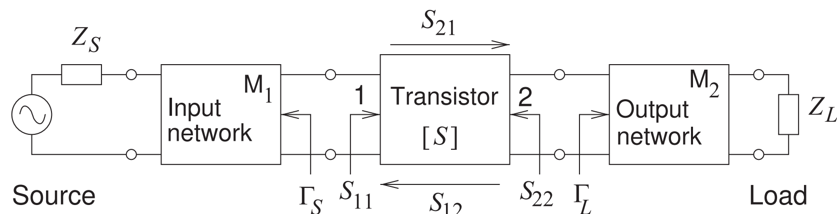
A linear amplifier can be represented as a two-port with a Thevenin equivalent source at Port 1 and a load at Port 2, as shown in Figure 2-4(a). This section illustrates the usefulness of generalized S parameters in working with power flow in systems with different system impedances at the ports. Let **S** be the normalized scattering matrix of the two-port, with Z_0 being the normalizing real characteristic impedance:

$$\mathbf{S} = [S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \tag{2.6}$$

The development in this section uses the normalized S parameters of the amplifier in Figure 2-4(a). The aim is to develop an expression for the



(a) An amplifier



(b) Active device with input and output matching networks

Figure 2-4: Two-port network with source and load used in defining unilateral gain measures.

unilateral transducer gain and for the maximum unilateral transducer gain. The unilateral transducer gain is restricted to the amplifier (Figure 2-4(a)), and the maximum unilateral transducer gain can use the S parameters of either the transistor (Figure 2-4(b)) or the amplifier (Figure 2-4(a)).

The generalized scattering matrix of the amplifier will be normalized to the source impedance, Z_S, and load impedance, Z_L, shown in Figure 2-4. First, the reflection coefficients Γ_S and Γ_L (normalized to Z_0) at the source and load are found using

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \quad \text{and} \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.7}$$

From Equation (2.132) of [2], the generalized scattering parameters (with Port 1 normalized to Z_S and Port 2 normalized to Z_L) are

$$^G\mathbf{S} = (\mathbf{D}^*)^{-1}(\mathbf{S} - \mathbf{\Gamma}^*)(\mathbf{U} - \mathbf{\Gamma}\mathbf{S})^{-1}\mathbf{D}, \tag{2.8}$$

where

$$\mathbf{\Gamma} = \begin{bmatrix} \Gamma_S & 0 \\ 0 & \Gamma_L \end{bmatrix}, \quad \mathbf{D} = \begin{bmatrix} D_{11} & 0 \\ 0 & D_{22} \end{bmatrix}, \tag{2.9}$$

$$D_{11} = \frac{(1-\Gamma_S)\sqrt{1-|\Gamma_S|^2}}{|1-\Gamma_S^*|} \quad \text{and} \quad D_{22} = \frac{(1-\Gamma_L)\sqrt{1-|\Gamma_L|^2}}{|1-\Gamma_L^*|}. \tag{2.10}$$

Following tedious algebraic manipulations, the following expressions are obtained:

$$^GS_{11} = \frac{1}{W}\frac{1-\Gamma_S}{1-\Gamma_S^*}[(S_{11}-\Gamma_S^*)(1-\Gamma_L S_{22}) + S_{12}S_{21}\Gamma_L] \tag{2.11}$$

$$^GS_{12} = \frac{1}{W}\frac{(1-\Gamma_S)(1-\Gamma_L)}{|1-\Gamma_S||1-\Gamma_L|}S_{12}[(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)]^{\frac{1}{2}} \tag{2.12}$$

$$^GS_{21} = \frac{1}{W}\frac{(1-\Gamma_S)(1-\Gamma_L)}{|1-\Gamma_S||1-\Gamma_L|}S_{21}[(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)]^{\frac{1}{2}} \tag{2.13}$$

$$^GS_{22} = \frac{1}{W}\frac{1-\Gamma_L}{1-\Gamma_L^*}[(S_{22}-\Gamma_L^*)(1-\Gamma_S S_{11}) + S_{12}S_{21}\Gamma_S], \tag{2.14}$$

where

$$W = (1-\Gamma_S S_{11})(1-\Gamma_L S_{22}) - S_{12}S_{21}\Gamma_S\Gamma_L \tag{2.15}$$

and

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = {}^G\mathbf{S}\begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{2.16}$$

Here a and b are the root power waves defined in Figure 2-17 of [2].

A number of useful observations can be made. First, in a matched condition where $\Gamma_S = \Gamma_L = 0$ (i.e., $Z_S = Z_L = Z_0$), $^G\mathbf{S} = \mathbf{S}$. Second, for a reciprocal two-port network with $S_{12} = S_{21}$, the generalized scattering parameters are also reciprocal (i.e., $^GS_{12} = {}^GS_{21}$). An amplifier is not reciprocal, however, and for a good amplifier, $^GS_{12}$ is approximately zero and $\left|^GS_{21}\right|$ is greater than one, indicating power gain.

Now the transducer power gain, G_T, can be expressed in terms of device S parameters. G_T (Equation (2.3)) is defined as the ratio of the average power, P_L, delivered to the load Z_L, and the maximum input power available from the generator, P_{Ai}, that is,

$$G_T = \frac{P_L}{P_{Ai}}, \tag{2.17}$$

where the available power from the generator is

$$P_{Ai} = \frac{1}{8}\frac{|V_S|^2}{\Re\{Z_S\}} = \frac{1}{2}|a_1|^2 \tag{2.18}$$

and the power delivered to the load is

$$P_L = \frac{1}{2}\Re\{Z_L\}| - I_2|^2 = \frac{1}{2}|b_2|^2. \tag{2.19}$$

These quantities are defined in terms of the root power waves a_1 and b_2 and these are related by the generalized S parameters. Thus the transducer gain

$$G_T = \left|\frac{b_2}{a_1}\right|^2 = |{}^G S_{21}|^2, \tag{2.20}$$

and so, using Equation (2.13),

$$G_T = |S_{21}|^2 \frac{(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - \Gamma_S S_{11})(1 - \Gamma_L S_{22}) - \Gamma_S \Gamma_L S_{12} S_{21}|^2}. \tag{2.21}$$

This combines the inherent voltage gain of the device (S_{21}) with the effect of load and source mismatches through Γ_L and Γ_S. This expression simplifies under particular circumstances that will now be considered.

If the source and load impedances are both equal to the system impedance, then the transducer gain becomes

$$G_T|_{Z_0} = |S_{21}|^2. \tag{2.22}$$

This is the transducer gain without matching networks, so that $\Gamma_S = 0 = \Gamma_L$. This is nearly always much lower than what can be achieved using matching networks. For one, an active device has significant input and output reactances at microwave frequencies that need to be tuned out.

For a unilateral two-port, $S_{12} = 0$ (and this is a reasonable approximation for many amplifiers, as there is little feedback from the output to the input). Then the transducer gain becomes the **unilateral transducer gain**, G_{TU}:

$$G_{TU} = |S_{21}|^2 \left(\frac{1 - |\Gamma_S|^2}{|1 - \Gamma_S S_{11}|^2}\right)\left(\frac{1 - |\Gamma_L|^2}{|1 - \Gamma_L S_{22}|^2}\right). \tag{2.23}$$

This is often referred to as just the **unilateral gain**.

From the last expression it can be seen that by choosing $\Gamma_S = (S_{11})^*$ and $\Gamma_L = (S_{22})^*$ (i.e., the complex conjugates), G_{TU} achieves its maximum value, the **maximum unilateral transducer gain**:

$$G_{TU\max} = |S_{21}|^2 \left(\frac{1}{1 - |S_{11}|^2}\right)\left(\frac{1}{1 - |S_{22}|^2}\right). \tag{2.24}$$

Frequency (GHz)	$G_{TU\max}$ (dB)
0.5	36.62
1	31.07
2	24.88
3	21.26
4	18.73
5	16.00
6	15.74
7	14.52
8	13.26
9	12.36
10	12.24
11	12.07
12	11.77
13	11.46

Frequency (GHz)	$G_{TU\max}$ (dB)
14	11.25
15	11.61
16	11.64
17	11.11
18	10.50
19	8.89
20	7.91
21	7.48
22	6.55
23	5.46
24	4.62
25	4.22
26	3.61

Table 2-1: Maximum unilateral transducer gain, $G_{TU\max}$, of the pHEMT transistor documented in Figure 2-2.

Note that up to now the S parameters have been those of the transistor, see Figure 2-4(b). So $G_{TU\max}$ is the maximum unilateral transducer gain available from the active device. This is a good measure of the maximum power gain readily obtained from the device. However, with feedback (consider the general amplifier configuration of Figure 2-17) the effective $S_{12} \neq 0$, and any gain can be achieved, even oscillation. Also, higher gain is obtained at the expense of reduced bandwidth. As a general design guideline, the closer the gain specified for an amplifier is to $G_{TU\max}$, the more challenging the design task.

The maximum unilateral transducer gain, $G_{TU\max}$, of the pHEMT transistor described in Figure 2-2 in shown in Table 2-1. The maximum unilateral transducer gain is largest at low frequencies and monotonically reduces as frequency increases. This means that it is difficult to design a broadband amplifier using a pHEMT (and this is true with most FETs). It is also a challenge to ensure stable amplification at low frequencies and matching networks must be chosen to suppress low-frequency gain.

The power gain with the input conjugately matched is

$$G_P = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{|(1-S_{22}\Gamma_L)(1-|S_{11}|^2)}, \tag{2.25}$$

and with $\Gamma_L = 0$,

$$G_P|_{\Gamma_L=0} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)}. \tag{2.26}$$

The available power gain with the output conjugately matched is

$$G_A = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|S_{22}|^2)}, \tag{2.27}$$

and with $\Gamma_S = 0$,

$$G_A|_{\Gamma_S=0} = \frac{|S_{21}|^2}{1-|S_{22}|^2}. \tag{2.28}$$

The maximum available power gain, $G_{\rm MA}$, equal to both G_A and G_T with optimum M_1 and M_2 is

$$G_{\rm MA} = \left|\frac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right), \tag{2.29}$$

where the **Rollet's stability factor** [3, 4]

$$k = \left(\frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}|\,|S_{21}|}\right) \quad \text{and} \quad \Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{2.30}$$

Rollett developed the expressions for $G_{\rm MA}$ and k in terms of z, y, and h parameters [3, 4]. The expressions in Equations (2.29) and (2.30) are developed using the equivalences given in Table 2-2 of [2].

$G_{\rm MA}$ is only defined when $k \geq 1$ indicating that if $k < 1$ the amplifier can be expected to oscillate if both M_1 and M_2 are optimized for maximum power transfer. Provided that $k \geq 1$, $G_{\rm MA}$ is the maximum gain that can be achieved without using feedback from the output of the active device to its input. It is still possible to obtain stable gain when $k < 1$ but it is necessary to use either nonoptimum M_1 or M_2, or feedback across the active device.

Another important gain metric is the maximum stable gain $G_{\rm MS}$ that can be achieved. Of course this is just $G_{\rm MA}$ if the amplifier is unconditionally stable. If $k < 1$, Rollett showed that the amplifier is potentially unstable (this will be discussed in greater detail in Section 2.6) [3, 4]. Then $G_{\rm MS}$ will be less than $G_{\rm MA}$. Rollett ensured stability of the amplifier by putting shunt admittances at the input and output ports of the transistor so that for the augmented transistor two-port $k = 1$. Then the maximum stable power gain, $G_{\rm MS}$, is $G_{\rm MA}$ in Equation 2.29 but with k set to 1:

$$G_{\rm MS} = \left|\frac{S_{21}}{S_{12}}\right|. \tag{2.31}$$

From Table 2-2 of [2] it is seen that $S_{21}/S_{12} = z_{21}/z_{12} = y_{21}/y_{12} = h_{21}/h_{12}$ so that the surprising result is that the maximum stable gain, a power gain, is the ratio of the forward parameter to the reverse parameter and not the square of the ratio, and those parameters could be S, z, y, or h parameters.

Experience indicates that $G_{\rm MS}$ is the practical limit to the stable gain that can be achieved with moderate design effort. (Note that the amplifier could be stable without being conditionally stable which is the criterion used in developing $G_{\rm MS}$, and schemes other than using shunt admittances could be used to achieve unconditional stability). $G_{\rm MS}$ is interpreted as the maximum gain that can be achieved while ensuring that the amplifier is unconditionally stable.

The final useful gain metric is the unilateral power gain, U. This is the maximum available gain, $G_{\rm MA}$, with feedback across the active device adjusted so that the effective device feedback parameter $S_{12} = 0$. When $U = 1$, the devices go from being active to being passive [5]:

$$U = \left(\frac{|S_{21}/S_{12} - 1|^2}{2k|S_{21}/S_{12}| - 2\Re(S_{21}/S_{12})}\right). \tag{2.32}$$

2.3.2 Design Using Gain Metrics

$G_{TU,\max}$, $G_{\rm MS}$, $G_{\rm MA}$, and U are used by designers as measures of the ultimate performance of a device and to guide design. They are important FOMs

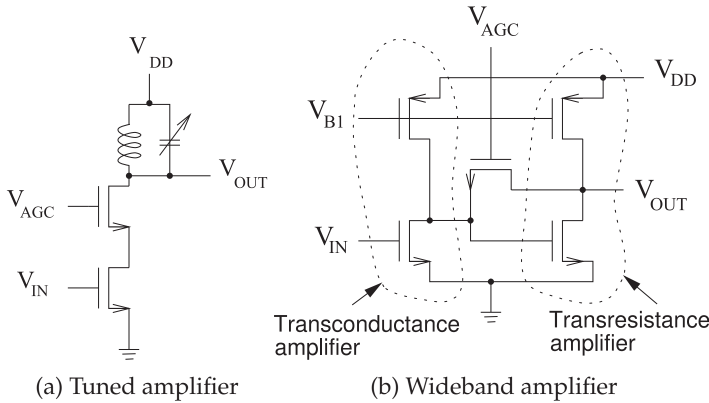


Figure 2-5: Low-noise amplifiers. $V_{\rm AGC}$ is the automatic gain control voltage and sets the gain of the amplifiers.

as they are defined with extreme conditions. Of these metrics only $G_{\rm MA}$ relates to the unaltered device S parameters. $G_{\rm MA}$ is the maximum gain that can be obtained with optimum input and output matching networks. If the amplifier is potentially unstable with optimum M_1 and M_2, then $G_{\rm MA}$ is undefined.

$G_{TU,\max}$ is the gain when the effective S_{12} is set to zero (perhaps using feedback) but instead of optimum M_1 and M_2, Γ_S is set to S_{11}^* and Γ_L is set to S_{22}^*. (S_{11} and S_{22} are those of the active device and are unaffected by feedback.) With $S_{12} = 0$, the choice for Γ_L is the same as using an optimum M_2. However the choice for Γ_S (i.e. $\Gamma_S = S_{11}^*$) is not the same as using an optimum M_1. Choosing an optimum M_1 would lead to a higher system gain (i.e., $G > G_{TU,\max}$). Experience is that $G_{TU,\max}$ can be achieved with little design effort. It is used primarily in initial choice of the active device.

$G_{\rm MS}$ and U are the maximum available gains for two different specific although artificial conditions. $G_{\rm MS}$ is the maximum available gain with k set 1, perhaps using feedback, but otherwise not changing the device's S parameters. Design experience is that $G_{\rm MS}$ is the stable gain that can be achieved with moderate design effort. U is the maximum available gain with S_{12} set to 1, perhaps using feedback, but otherwise not changing the device's S parameters. The design experience is that U indicates the highest frequency at which gain can be achieved and this is when $U = 1$.

$G_{TU,\max}$, $G_{\rm MS}$, $G_{\rm MA}$, and U are tabulated in Table 2-2 for the pHEMT transistor documented in Figure 2-2. As will be shown in Section 2.6.3, the amplifier is unconditionally stable from 5 to 11 GHz and above 22 GHz. Outside those ranges, matching networks can be chosen so that the amplifier could oscillate and then $G_{\rm MA}$ is not defined. $G_{\rm MS}$ is usually taken as the highest gain that can be easily achieved. However, higher gains can be achieved with more attention to stability, but then usually amplification is available only over a very narrow bandwidth.

Once a design is completed, the only gain that matters is the transducer gain, G_T, which is the ratio of the power delivered to a load to the power available from the source.

2.3.3 Gain Circles

The expressions for gains developed in Section 2.3.1 were in terms of absolute values of complex numbers. It is therefore possible to present gains at a particular frequency using circles on the complex reflection coefficient

Table 2-2: Device gain metrics for the pHEMT transistor in Figure 2-2.

Freq. (GHz)	Max. unilateral transducer gain $G_{TU,\max}$ (db)	Max. available power gain G_{MA} (db)	Max. stable power gain G_{MS} (db)	Unilateral power gain U (db)
0.5	36.6	–	30.1	41.9
1	31.1	–	27.1	39.4
2	24.9	–	24.2	34.4
3	21.3	–	22.4	29.7
4	18.7	–	21.3	25.6
5	17.0	18.6	20.4	23.6
6	15.7	17.0	19.6	22.6
7	14.5	15.5	18.7	20.8
8	13.6	14.0	18.2	17.9
9	12.4	13.0	17.7	16.4
10	12.2	13.2	16.6	17.8
11	12.1	13.7	15.7	19.5
12	11.8	–	14.8	20.5
13	11.5	–	14.2	20.5
14	11.2	–	13.5	21.2
15	11.6	–	13.1	27.6
16	11.6	–	12.7	24.2
17	11.1	–	12.3	21.4
18	10.5	–	11.9	17.0
19	8.88	–	11.5	12.9
20	7.91	–	11.2	11.4
21	7.48	–	10.9	11.0
22	6.55	8.42	10.4	9.22
23	5.46	6.62	9.97	7.43
24	4.62	5.55	9.62	6.22
25	4.23	5.17	9.05	5.73
26	3.61	4.27	8.57	4.79

plane [6]. The mathematics behind this are developed in Section 1.A.13 of [7].

Two of the more useful gains to use in making trade-offs are the maximum available gain G_{MA} (Equation (2.29)) and the maximum stable gain G_{MS} (Equation (2.31)). G_{MA} is the available G_A and G_T with optimum M_1 and M_2, but only has a finite value when the transistor is unconditionally stable. Microwave circuit simulators use another gain measure to handle this situation. If a transistor is conditionally stable then resistive loading is used to ensure unconditional stability. So the maximum available gain calculated in microwave simulators is G_{MA} if it has a finite value but is G_{MS} otherwise. Introducing G_{MAX} to describe this gain:

$$G_{\text{MAX}} = \begin{cases} G_{\text{MA}} = \left|\dfrac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right) & \text{if } k \geq 1 \\ \\ G_{\text{MS}} = \left|\dfrac{S_{21}}{S_{12}}\right| & \text{if } k < 1 \end{cases} . \tag{2.33}$$

Here k is Rollet's stability factor (see Equation (2.30).

The discussion can now turn to defining gain circles. Gain circles plot the locus of the available power gain, G_A, as defined in Equation (2.27), on the input reflection coefficient, Γ_S, plane. G_A is a function of the magnitude of complex numbers and so circles can be defined in the complex plane. Figure

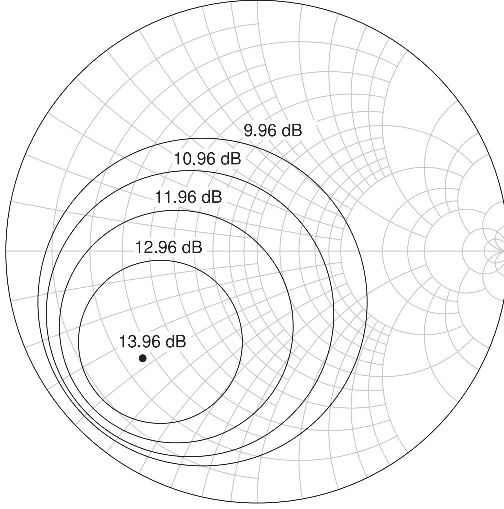


Figure 2-6: Gain circles of the transistor in Figure 2-2 at 8 GHz plotted on the Γ_S plane.

2-6 plots the G_A gain circles for the pHEMT transistor at 8 GHz on the input reflection coefficient plane. The center of the family of circles is G_{MAX} and this point defines the Γ_S value required to achieve G_{MAX}. The other circles moving out plot the locus of Γ_S for reductions of available power gain, G_A, in 1 dB steps below G_{MAX}. That is, a circle defines the values of Γ_S that will yield a specific G_A.

2.4 Amplifier Efficiency

There are several ways of expressing amplifier efficiency depending on how the RF input power is treated. One measure of efficiency of a circuit is the useful output power divided by the input power, and considers the contribution of the RF input power. This measure of efficiency is called **power-added efficiency** (**PAE**). At RF and microwave frequencies, the most common definition of PAE used with power amplifiers focuses on the additional RF power divided by the DC input power. Thus

$$\eta_{\text{PAE}} = \frac{P_{\text{RF,out}} - P_{\text{RF,in}}}{P_{\text{DC}}}. \tag{2.34}$$

There is another definition of PAE, but it is less commonly used at RF and microwave frequencies [8]. However, this alternative definition can be used with any two-port network. RF and microwave circuit designers refer to this as the **total power-added efficiency** and at lower frequencies it is called the **transmit chain efficiency**. This efficiency is denoted η_{total} and is defined as

$$\eta_{\text{total}} = \frac{P_{\text{RF,out}}}{P_{\text{DC}} + P_{\text{RF,in}}}. \tag{2.35}$$

RF engineers also refer to this as the **overall amplifier efficiency**:

$$\eta_{\text{overall}} = \eta_{\text{total}} = \frac{P_{\text{RF,out}}}{P_{\text{DC}} + P_{\text{RF,in}}}. \tag{2.36}$$

A final definition is the **average amplifier efficiency**, η_{avg} [9]. This metric takes into account the time-varying level of a modulated communications

Table 2-3: Comparison of efficiency metrics for an amplifier producing 1 W RF output power and consuming 2 W of DC power with various power gains.

Power gain (dB)	$\eta_{\rm TOTAL}$	$\eta_{\rm PAE}$	η_D
3	40%	25%	50%
6	44%	37%	50%
10	48%	45%	50%
15	49%	48%	50%
20	50%	50%	50%
40	50%	50%	50%

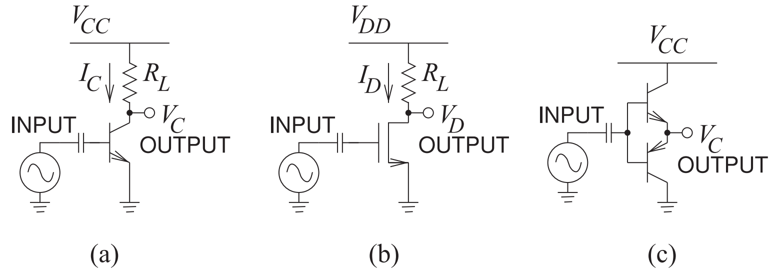


Figure 2-7: Class A single-ended resistively biased amplifiers: (a) BJT transistor with B for base terminal, C for collector terminal, and E for emitter terminal; (b) MOSFET transistor with G for gate terminal, D for drain terminal, and S for source terminal; and (c) Class B or Class C push-pull amplifier.

signal and is the ratio of the average RF output power to the average DC input power:

$$\eta_{\rm avg} = \frac{P_{\rm RF,out,avg}}{P_{\rm DC,avg}}. \tag{2.37}$$

For high-gain amplifiers, $P_{\rm RF,in} \ll P_{\rm DC}$, and all of the efficiencies become approximately equivalent and is simply called the **efficiency**, η, of the amplifier:

$$\eta = \frac{P_{\rm RF,out}}{P_{\rm DC}} \approx \eta_{\rm PAE} \approx \eta_{\rm total} \approx \eta_{\rm avg} \approx \eta_{\rm overall} \quad \text{(high gain)}. \tag{2.38}$$

When the primary input DC power is fed to the drain of a FET, the term **drain efficiency**, η_D, is used:

$$\eta_D = \frac{P_{\rm RF,out}}{P_{\rm DC}}. \tag{2.39}$$

This term is also used when the device is a BJT or HBT, although the term **collector efficiency** would be more appropriate.

The efficiency metrics are compared in Table 2-3 for an amplifier with 1 W RF output power. The first amplifier has a power gain of 3 dB, which is commonly the gain of the final amplifier stage producing the maximum output power available from a particular transistor technology.

2.5 Class A, AB, B, and C Amplifiers

Transistor amplifiers use several different biasing strategies. The strategies are identified as classes of amplifiers ranging from Class A to Class G. In this section Class A, AB, B, and C amplifiers are considered and these have the basic topologies of Figure 2-7, where input and output matching networks have been omitted. Class A–C amplifiers have the same impedance presented to the output of the amplifier at the operating frequency and at

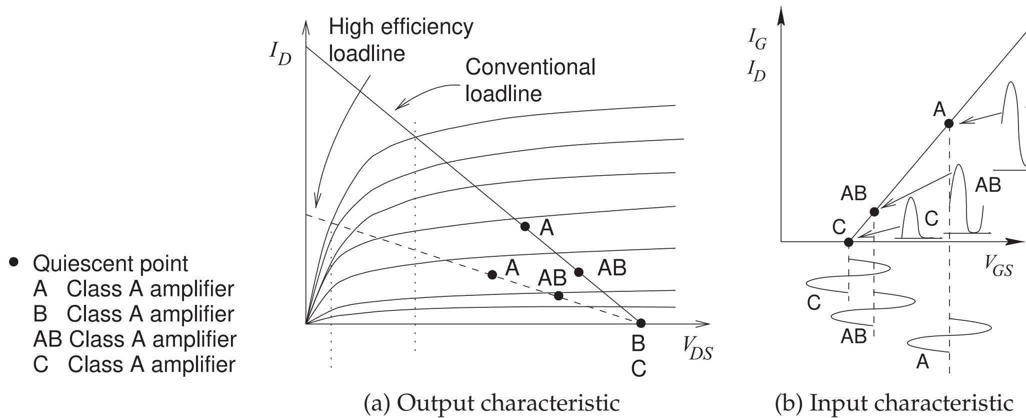


Figure 2-8: Current-voltage characteristics of a transistor used in an amplifier showing the quiescent points of various amplifier classes.

harmonics. Figure 2-8(a) is the output characteristic of a transistor and shows the distinguishing quiescent points for the various classes of amplifier. The input characteristics are shown in Figure 2-8(b), where the input (I_G) and output (I_D) current waveforms are shown for a sinusoidal input waveform (V_{GS}).

Amplifier design consists of both design for low-power linear operation, requiring maximum power transfer at the input and output of the amplifier, and a trade-off of acceptable distortion and efficiency. In practice, a certain level of distortion must be tolerated, and what is acceptable is embedded in the specifications of the various wireless systems.

For low distortion, the peaks of the RF signal must be amplified linearly, however, the DC power consumed depends on the amplifier class. With Class A amplifiers, the DC power must be sufficient to provide low-level distortion of the largest RF signal so that the DC power is proportional to the peak AC power.

The situation is similar for Class AB amplifiers, with the difference being that the intent is to accept some distortion of the peak signal so that the relationship between peak power and DC power still exists, but the direct proportionality no longer holds. For Class C and higher class amplifiers, the DC power is mostly proportional to the average RF power. So for Class A and Class AB amplifiers, the average operating point must be "backed off" to allow for manageable distortion of the peaks of a signal, with the level of back-off required being proportional to the PMEPR of the modulated signal. For Class C and higher classes, the back-off required comes from experience and experimentation. The characteristics of the signal also determine how much distortion can be tolerated.

The PMEPR of the signal is an indication of the type and amount of distortion that can be tolerated. The PMEPR of the two-tone signal is 3 dB, and digitally modulated signals can have PMEPRs ranging from 0 dB to 20 dB or more. A signal with a higher PMEPR results in lower efficiency, as more back-off is required. Putting this another way, the DC bias must be set so that there is minimum distortion when the signal is at its peak, but

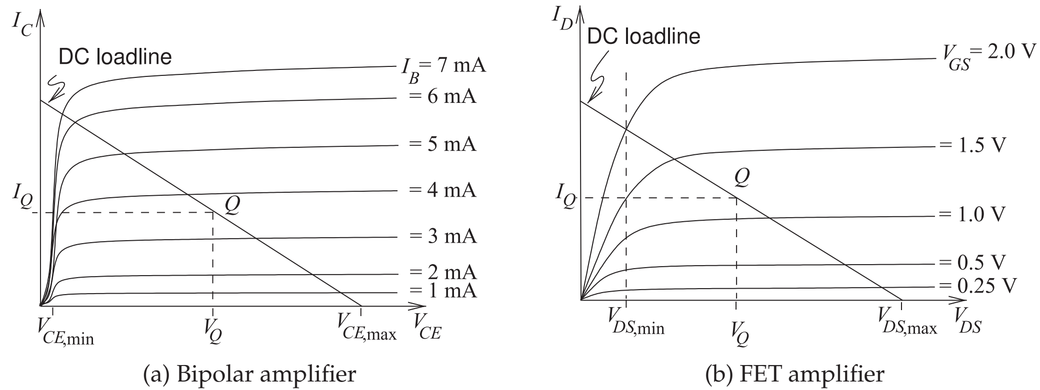


Figure 2-9: Current-voltage characteristics of transistor amplifiers shown with a Class A amplifier loadline: (a) bipolar amplifier; and (b) FET amplifier.

the average RF power produced can be much less than the peak RF power. (The average RF power is approximately an amount PMEPR below the peak RF power.) Thus for a high-PMEPR signal, generally a higher DC power is required to produce the same RF power. This is especially true for Class A amplifiers.

2.5.1 Class A Amplifier

The Class A amplifier has limited efficiency because there is always substantial quiescent current flowing whether or not RF current is flowing. Higher-order classes of amplifiers achieve higher efficiency, but distort the RF signal. The current and voltage loci of Class A, B, AB, and C amplifiers have a similar trajectory on the output current-voltage characteristics of a transistor. The output characteristics of a transistor are shown in Figure 2-8(a), showing what is called the linear or DC loadline and the bias points for the various amplifier classes. The loadline is the locus of the DC current and voltage as the DC input voltage is varied.

With the Class A amplifier, the transistor is biased in the middle of the transistor characteristics, where the response has the highest linearity. That is, when the gate voltage varies due to an applied signal, the output voltage and current variations are nearly linearly proportional to the applied input. The drawback is that there is always considerable DC current flowing, even when the input signal is very small. That is, there is DC power consumption whether or not RF power is being generated at the output of the transistor. This is not of concern if small RF signals are to be amplified, as then a small transistor can be chosen so that the DC current levels are small. It is a problem if an amplifier must handle both large and small signals.

The Class A amplifier is defined by its ability to amplify small to medium and even large signals with minimal distortion. This is achieved by biasing a transistor in the middle of its I-V (i.e., current-voltage) characteristics. Figure 2-9 shows the I-V characteristics of the bipolar and FET transistors shown in Figure 2-7, together with the DC loadline. The loadline is the locus of the output current and voltage. For the Class A amplifiers in Figure 2-7(a and b)

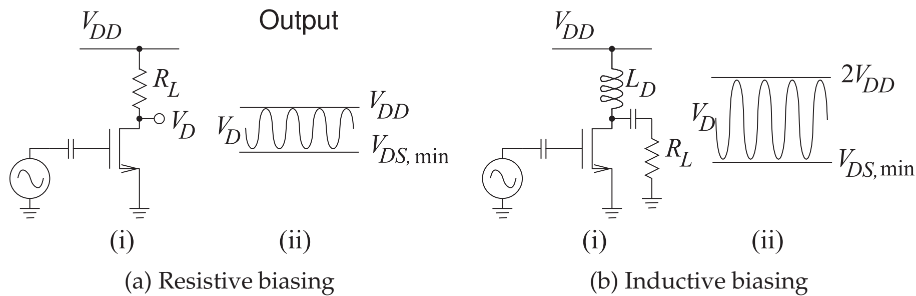


Figure 2-10: Single-ended Class A MOSFET amplifiers: (i) schematic; and (ii) drain voltage waveforms.

the loadlines are defined by

$$I_C = (V_{CC} - V_{CE})/R_L \quad \text{and} \quad I_D = (V_{DD} - V_{DS})/R_L \tag{2.40}$$

respectively. These are called single-ended amplifiers, as the input and output voltages are referred to ground. An amplifier using a bipolar transistor (either a BJT or an HBT), as shown in Figure 2-7(a), has the output characteristics shown in Figure 2-9(a). Here the output voltage of the bipolar amplifier is V_{CE}, and this swings from a maximum value of $V_{CE,\max}$ to a minimum of $V_{CE,\min}$. For a bipolar transistor $V_{CE,\min}$ is approximately 0.2 V, while $V_{CE,\max}$ for a resistively biased circuit is just the supply voltage, V_{CC}. The quiescent or bias point is shown with collector-emitter voltage V_Q and quiescent current I_Q. For a Class A amplifier, the quiescent point is just the bias point, and this is in the middle of the output voltage swing and the slope of the loadline is established by the load resistor, R_L.

The output I-V characteristic of a FET amplifier is shown in Figure 2-9(b). The notable difference between these characteristics and those of the bipolar transistor is that the curves are less abrupt at low output voltage (i.e., low V_{DS}). This results in the FET amplifier's minimum output voltage, $V_{DS,\min}$, being larger than that of a BJT-based amplifier, $V_{CE,\min}$. For a typical RF FET amplifier, $V_{DS,\min}$ is 0.5 V.

The bipolar and FET amplifiers of Figure 2-7 use resistive biasing so that the maximum output voltage swing is limited. As well, the bias resistor is also the load resistor. Various alternative topologies have been developed yielding a range of output voltage swings. The common variations are shown in Figure 2-10 for a FET amplifier. Figure 2-10(a) is a resistively biased Class A amplifier with the output voltage swing between $V_{DS,\min}$ and V_{DD}. The quiescent drain-source voltage is halfway between these extremes. The load, R_L, also provides correct biasing. A more efficient Class A amplifier uses inductive biasing, as shown in Figure 2-10(b). Bias current is now provided via the drain inductor, and the load, R_L, is not part of the bias circuit. With the inductively loaded Class A amplifier, the quiescent voltage is V_{DD} and the output voltage swing is between $V_{DS,\min}$ and $2V_{DD}$, slightly more than twice the voltage swing of the resistively loaded amplifier.

A Class A amplifier can be designed using the S parameters of the transistor in a specific configuration. Ideally the effect of bias circuitry would be included in the S parameters of the transistor, but bias circuit

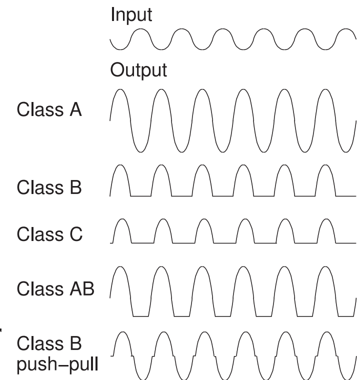


Figure 2-11: Input and output waveforms for various classes of amplifier.

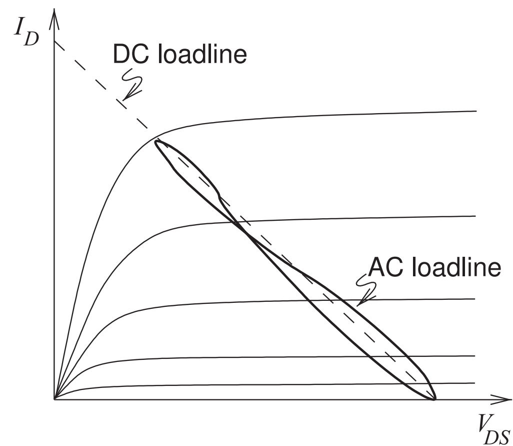


Figure 2-12: DC and RF loadlines of Class A, B, and C amplifiers. The AC loadline is also called the dynamic loadline.

design attempts to present RF open or short circuits as required to minimize impact on RF performance. Generally design begins with the transistor's S parameters and assuming no bias circuit impact.

2.5.2 Amplifier Efficiency

Since the Class A amplifier is always drawing DC current, its efficiency is near zero when the input signal is very small. The maximum efficiency of Class A amplifiers is 25% if resistive biasing is used and 50% when inductive biasing is used. Efficiency is improved by reducing the DC power, and this is achieved by moving the bias point further down the DC loadline, as in the Class B, AB, and C amplifiers shown in Figure 2-8. Reducing the bias results in signal distortion for large RF signals. This can be seen in the various output waveforms shown in Figure 2-11. Class A amplifiers have the highest linearity and Class B and C amplifiers result in considerable distortion. As a compromise, Class AB amplifiers are used in many cellular applications, although Class C amplifiers are used with constant envelope modulation schemes, as in GSM. Nearly all small-signal amplifiers are Class A.

The effect of parasitic capacitances and delay effects (such as those due to the time it takes carriers to move across a base for a BJT or under the gate for a FET) result in the current-voltage locus for RF signals differing from the DC situation. This effect is captured by the **dynamic or AC loadline**, which is shown in Figure 2-12.

The Class A amplifier is a low-efficiency, but highly linear class. The other

amplifier classes have higher efficiencies but varying degrees of distortion, as seen in Figure 2-11. The output of the Class B amplifier contains an amplified version of only half of the input signal but draws just a small leakage current when no signal is applied. With the Class C amplifier there must be some positive RF input signal before there is an output: there is more distortion but no current flows, not even leakage current, when there is no RF input signal. The Class AB amplifier is a compromise between Class A and Class B amplifiers. Less DC current flows than with Class A when there is negligible input signal, and the distortion is less than with Class B. Filtering, often provided by matching networks, eliminates harmonics from the output of the amplifier, but in-band distortion of finite bandwidth signals remains.

Class C amplifiers are biased so that there is almost no drain-source (or collector-emitter) current when no RF signal is applied, so the output waveform has considerable distortion, as shown in Figure 2-11. This distortion is important only if there is information in the amplitude of the signal. FM, PM, and to a lesser extent GMSK schemes result in signals with constant (or for GMSK near constant) RF envelopes, thus there is no information contained in the amplitude of the signal. Therefore errors introduced into the amplitude of a signal are of lesser significance and efficient saturating mode amplifiers such as a Class C amplifier can be used. In contrast, PSK and QAM modulation schemes do not result in signals with constant RF envelopes and so some information is contained in the amplitude of the RF signal. For these modulation techniques, reasonably linear amplifiers are required.

The Class A amplifier presents input and output impedances that are almost independent of the level of the signal. However, a Class B, AB, or C amplifier presents input and output impedances that vary depending on the level of the RF signal. Thus design requires more care, as the chances of instability are higher and it is more likely that an oscillation condition will be met. Also, Class B, AB, and C amplifiers are generally not used in broadband applications or at high frequencies (say above 20 GHz) mainly because of the problem of maintaining stability. Class A amplifiers are then the preferred solution as design is simpler and the amplifier is more tolerant of parasitic effects and variations.

EXAMPLE 2.2 Efficiency of a Class A Amplifier

Determine the efficiency of a Class A FET amplifier with resistive biasing using the FET characteristics shown in Figure 2-9(b).

Solution:

For maximum output voltage swing, the quiescent point should be halfway between the maximum and minimum drain source voltages,

$$V_O = V_{DS,\mathrm{min}} + \left(\frac{V_{DS,\mathrm{max}} - V_{DS,\mathrm{min}}}{2}\right) = \left(\frac{V_{DD} + V_{DS,\mathrm{min}}}{2}\right), \tag{2.41}$$

since $V_{DS,\mathrm{max}} = V_{DD}$. The quiescent (DC) current through R_L is

$$I_Q = \frac{V_{DD} - V_O}{R_L} = \left(V_{DD} - \frac{V_{DD} + V_{DS,\mathrm{min}}}{2}\right)\frac{1}{R_L} = \frac{V_{DD} - V_{DS,\mathrm{min}}}{2R_L}, \tag{2.42}$$

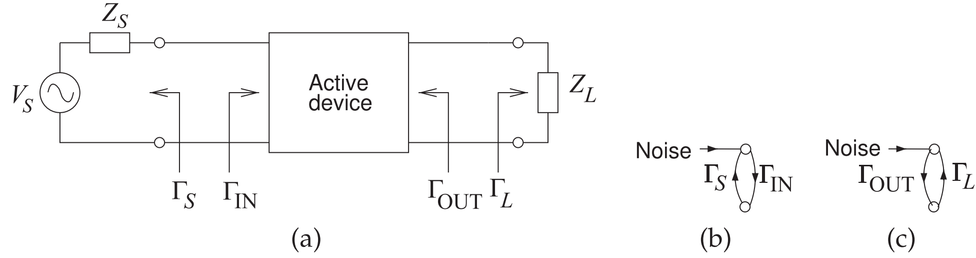


Figure 2-13: A two-port network with inputs at the source and load used in defining stability measures: (a) network; (b) input signal flow graph; and (c) output signal flow graph.

and the quiescent (DC) power consumed is

$$P_{DC} = V_{DD}I_Q = V_{DD}\left(\frac{V_{DD} - V_{DS,\text{min}}}{2R_L}\right) = \frac{V_{DD}^2}{2R_L}\left(1 - \frac{V_{DS,\text{min}}}{V_{DD}}\right). \tag{2.43}$$

The peak voltage of the AC output is

$$V_p = (V_{DD} - V_{DS,\text{min}})/2, \tag{2.44}$$

so that the RF output power in the load is

$$P_{RF,\text{out}} = \frac{1}{2}\left(\frac{V_{DD} - V_{DS,\text{min}}}{2}\right)^2 \frac{1}{R_L} = \frac{V_{DD}^2}{8R_L}\left(1 - \frac{V_{DS,\text{min}}}{V_{DD}}\right)^2. \tag{2.45}$$

Thus the efficiency of the amplifier is

$$\eta = \frac{P_{RF,\text{out}}}{P_{DC}} = \frac{1}{4}\left(1 - \frac{V_{DS,\text{min}}}{V_{DD}}\right). \tag{2.46}$$

If the minimum drain voltage is ignored ($V_{DS,\text{min}} = 0$), then $\eta = 1/4 = 25\%$. This is the maximum efficiency of a resistively biased Class A amplifier.

2.6 Amplifier Stability

The potential exists for an amplifier to be unstable and oscillate. Generally this is not a constant oscillation with fixed amplitude and frequency, but a chaotic response. Oscillator design is not as simple as designing an unstable amplifier, if only one could be so lucky. There is not a simple metric that will indicate whether an amplifier will be stable or not. In the worst case a transistor will oscillate no matter what is done to the external circuitry [10]. A manufacturer could not sell such a transistor and it would not be a useful component in a monolithic integrated process. So it is not surprising that stable amplifiers can be designed using available transistors. For stability analysis, the active device in a linear amplifier can often be treated as a two-port (see Figure 2-13(a)).

Stability considerations affect the maximum (stable) gain that can be achieved and the ease of design. If the maximum stable gain is too low then another transistor needs to be selected. If the specified gain is close to the maximum stable gain, then design will be challenging, especially for broader

bandwidths. So design effort increases with simpler (and hence cheaper) transistors. Experience is the best guide to making this tradeoff.

There are many ways of looking at stability. In the time-domain instability is manifested as the growth of signals over time independent of the level of the input signal. However it is most efficient to analyze and design RF and microwave circuits in the frequency domain and so stability must be assessed in the frequency domain as well. The many frequency domain techniques available to assess stability vary by the level of coverage and ease by which they can be applied. The simplest and most easily applied technique is based on two-port analysis, which leads to stability metrics based on two-port S parameters and to the concept of regions (called circles) of stability on a Smith chart and a more general technique is Nyquist stability analysis. These are considered below.

2.6.1 Two-Port Stability Analysis

Stability analysis should be applied to the innermost two-port containing the active device and any feedback networks. If the innermost two-port (including any feedback) is unconditionally stable, then the amplifier in which it is embedded will be stable. Thus there is a natural selection process so that available transistors tend to not suffer from internal instabilities.

Oscillation will initiate if signals reflected at the input port increase in amplitude as the signal reflects first from the source, Γ_S, and then from the input port. That is, if

$$|\Gamma_S \Gamma_{\text{IN}}| > 1, \tag{2.47}$$

the amplifier will be potentially unstable at the input. Whether or not it is actually unstable will depend on the phases of Γ_S and Γ_{IN}. This situation is shown in the signal flow graph of Figure 2-13(b), where oscillation is initiated by noise. Similarly oscillation will occur if multiple reflections between the output and the load build in amplitude. That is, if

$$|\Gamma_L \Gamma_{\text{OUT}}| > 1, \tag{2.48}$$

with the oscillation initiated by noise as shown in Figure 2-13(c). Now

$$|\Gamma_{\text{IN}}| = \left| S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \right| \tag{2.49}$$

and $$|\Gamma_{\text{OUT}}| = \left| S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \right|. \tag{2.50}$$

Combining Equations (2.47)–(2.50), the amplifier will be unstable if

$$|\Gamma_S \Gamma_{\text{IN}}| = \left| \Gamma_S S_{11} + \frac{S_{12} S_{21} \Gamma_S \Gamma_L}{1 - S_{22} \Gamma_L} \right| > 1 \tag{2.51}$$

or $$|\Gamma_L \Gamma_{\text{OUT}}| = \left| \Gamma_L S_{22} + \frac{S_{12} S_{21} \Gamma_S \Gamma_L}{1 - S_{11} \Gamma_S} \right| > 1. \tag{2.52}$$

The coupling of Γ_S and Γ_L makes it difficult to independently design the input and output matching networks. It is much more convenient to consider the **unconditionally stable** situation whereby the input is stable no matter

what the load and output matching network present, and the output is stable no matter what the source and input matching network present. As a first stage in design, a linear amplifier is designed for unconditional stability. The design space is larger if the more rigorous test for stability, embodied in Equations (2.51) and (2.52), is used to determine stability. The advantage (i.e., a larger design space), however, is often small.

If the source and load are passive, then $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$ so that oscillations will build up if

$$|\Gamma_{\rm IN}| > 1 \quad \text{and} \quad |\Gamma_{\rm OUT}| > 1. \tag{2.53}$$

For guaranteed stability for all passive source and load terminations (i.e., unconditional stability), then

$$|\Gamma_{\rm IN}| < 1 \quad \text{and} \quad |\Gamma_{\rm OUT}| < 1. \tag{2.54}$$

Amplifiers are often realized as stages whereby one amplifier stage feeds another. This complicates stability analysis, as it is possible for Γ_S and Γ_L to be more than unity. If Γ_S and Γ_L are both less than one for multiple amplifier stages, then the amplifier stability being described here can be used.

For the stability criteria to be used in design they must be put in terms of the scattering parameters of the active device. There are two suitable stability criteria commonly used, the k-factor and the μ-factor, which will now be considered.

2.6.2 Unconditional Stability: Two-Port Stability Circles

The input reflection coefficient of an active device is determined by the S parameters of the device and the load:

$$\Gamma_{\rm IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \tag{2.55}$$

and so for stability (for $|\Gamma_S| \leq 1$)

$$|\Gamma_{\rm IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1. \tag{2.56}$$

Similarly, considering the output of the active device, for stability (with $|\Gamma_L| \leq 1$),

$$|\Gamma_{\rm OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1. \tag{2.57}$$

Equations (2.56) and (2.57) must hold for all

$$|\Gamma_S| \leq 1 \quad \text{and} \quad |\Gamma_L| \leq 1. \tag{2.58}$$

When the active is unilateral, $S_{12} = 0$, and Equations (2.56) and (2.57) simplify to the requirement that $|S_{11}| < 1$ and $|S_{22}| < 1$. Otherwise, given a device, there will be a limit on the values of Γ_S and Γ_L that will ensure stability. The stability criteria are in terms of the magnitudes of complex numbers, and this is known to specify circles in the complex plane. The following development will lead to the center and radius defining the

stability circles that define the boundaries between stable and potentially unstable regions.

For $|\Gamma_{\mathrm{IN}}| = 1$, the output stability circle is defined by

$$\left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1. \tag{2.59}$$

The development that follows puts this into the standard form for a circle, that is, in the form of

$$|\Gamma_L - c| = r, \tag{2.60}$$

where c is a complex number and defines the center of the circle on a reflection coefficient plot, and r is a real number and is the radius of the circle. This circle defines the boundary between stable and potentially unstable values of Γ_L. Now Equation (2.59) can be rewritten as

$$|S_{11} - (S_{11}S_{22} - S_{12}S_{21})\Gamma_L| = |1 - S_{22}\Gamma_L|, \tag{2.61}$$

which includes the determinant, Δ, of the scattering parameter matrix. With

$$\Delta = S_{11}S_{22} - S_{12}S_{21}, \tag{2.62}$$

Equation (2.61) becomes

$$|S_{11} - \Delta\Gamma_L| = |1 - S_{22}\Gamma_L|. \tag{2.63}$$

Removing the absolute signs by multiplying each side by its complex conjugate and then rearranging,

$$(S_{11} - \Delta\Gamma_L)(S_{11} - \Delta\Gamma_L)^* = (1 - S_{22}\Gamma_L)(1 - S_{22}\Gamma_L)^* \tag{2.64}$$

$$S_{11}S_{11}^* + \Delta\Delta^*\Gamma_L\Gamma_L^* - (\Delta\Gamma_L S_{11}^* + \Delta^*\Gamma_L^* S_{11}) = 1 + S_{22}S_{22}^*\Gamma_L\Gamma_L^* - (S_{22}\Gamma_L + S_{22}^*\Gamma_L^*) \tag{2.65}$$

$$\left(|S_{22}|^2 - |\Delta|^2\right)\Gamma_L\Gamma_L^* - (S_{22} - \Delta S_{11}^*)\Gamma_L - (S_{22}^* - \Delta^* S_{11})\Gamma_L^* = |S_{11}|^2 - 1 \tag{2.66}$$

$$\Gamma_L\Gamma_L^* - \frac{(S_{22} - \Delta S_{11}^*)\Gamma_L}{|S_{22}|^2 - |\Delta|^2} - \frac{(S_{22} - \Delta S_{11}^*)^*\Gamma_L^*}{|S_{22}|^2 - |\Delta|^2} = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2}. \tag{2.67}$$

Adding the same term to both sides,

$$\Gamma_L\Gamma_L^* - \frac{(S_{22} - \Delta S_{11}^*)\Gamma_L}{|S_{22}|^2 - |\Delta|^2} - \frac{(S_{22} - \Delta S_{11}^*)^*\Gamma_L^*}{|S_{22}|^2 - |\Delta|^2} + \frac{(S_{22} - \Delta S_{11}^*)(S_{22} - \Delta S_{11}^*)^*}{\left(|S_{22}|^2 - |\Delta|^2\right)^2} = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2} + \frac{(S_{22} - \Delta S_{11}^*)(S_{22} - \Delta S_{11}^*)^*}{\left(|S_{22}|^2 - |\Delta|^2\right)^2} \tag{2.68}$$

and collecting terms leads to the equation for a circle:

$$\left| \Gamma_L - \frac{S_{22} - \Delta S_{11}^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|. \tag{2.69}$$

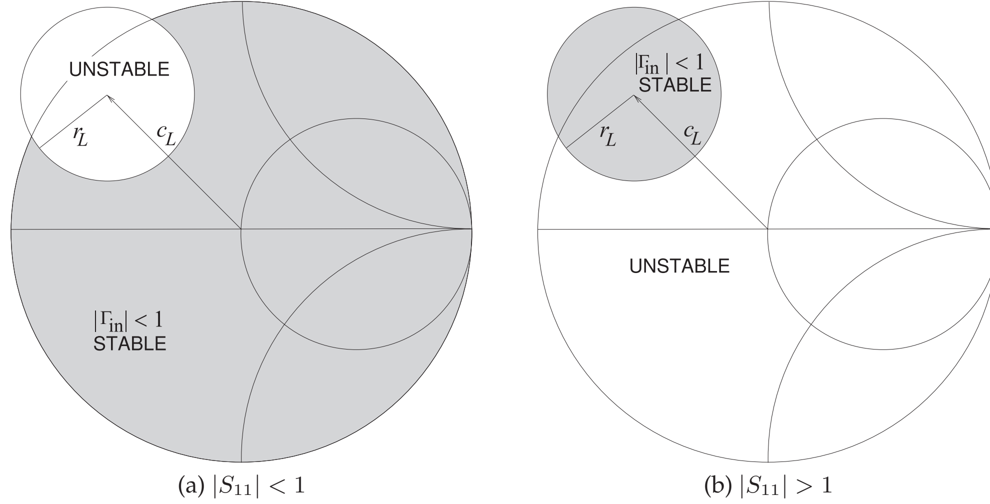


Figure 2-14: Output stability circles on the Γ_L plane. The shaded regions denote the values of Γ_L that will result in unconditional stability at the input indicated by $|\Gamma_{\rm in}| < 1$.

This defines a circle, called the output stability circle, in the Γ_L plane with center c_L and radius r_L (the development of this is given in Section 1.A.13) of [7]:

$$\text{center}: \; c_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad (2.70) \qquad \text{radius}: \; r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|. \quad (2.71)$$

This circle is plotted on a Smith chart in Figure 2-14 for the two conditions $|S_{11}| < 1$ and $|S_{11}| > 1$. When $|S_{11}| < 1$ the shaded region in Figure 2-14(a) indicates unconditional stability. That is, as long as Γ_L is chosen to lie in the shaded region, the input reflection coefficient, $\Gamma_{\rm in}$, will be less than one. It does not matter what the source impedance is, as long as it is passive there will not be oscillation due to multiple reflections between the input of the amplifier and the source.

Similarly an input stability circle can be defined for Γ_S, where

$$\text{center}: \; c_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad (2.72) \qquad \text{radius}: \; r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|. \quad (2.73)$$

The interpretation of the input stability circles, shown in Figure 2-15, is similar to that for the output stability circles.

The stability criterion provided by the input and output stability circles is very conservative. For example, the input stability circle (for Γ_S) indicates the value of Γ_S that will ensure stability no matter what passive load is presented. Thus the stability circles here are called unconditional stability circles. However, an amplifier can be stable for loads (or source impedances) other than those that ensure unconditional stability. The use of stability circles provides a good first pass in design of the matching networks between the actual source and load and the amplifier. The stability circles will change with frequency, and so ensuring stability requires a broad frequency view. This is considered in the linear amplifier design case study in Section 2.9.

Shading is commonly used in publications to indicate the stable and

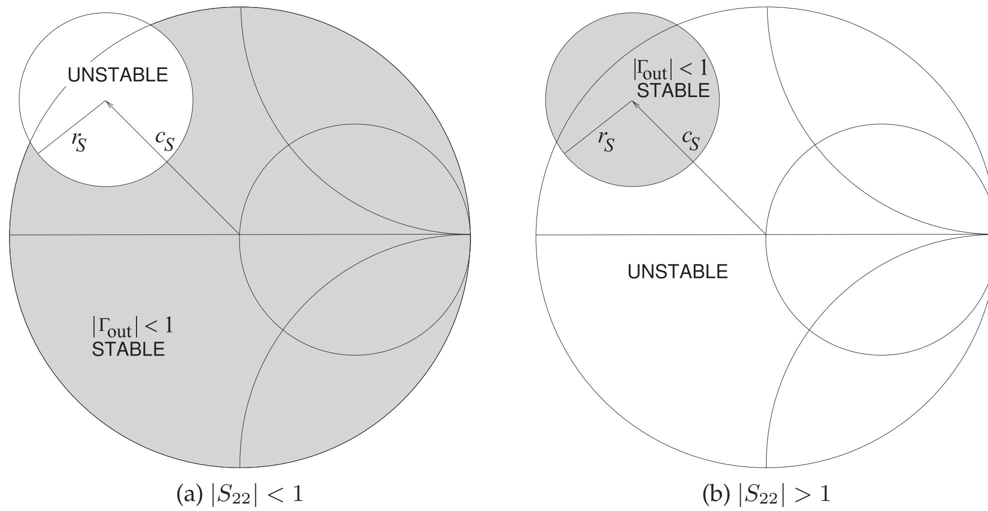


Figure 2-15: Input stability circles on the Γ_S plane. The shaded regions denote the values of Γ_S that will result in unconditional stability at the output indicated by $|\Gamma_{\text{out}}| < 1$.

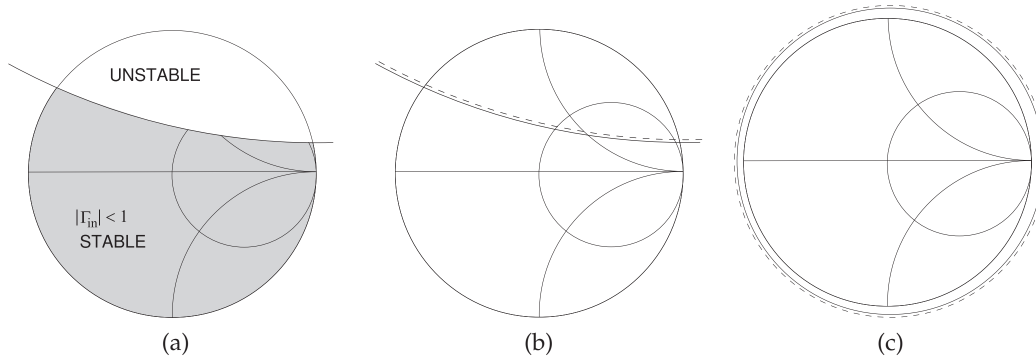


Figure 2-16: Stability circles: (a) using the absence of shading to indicate the potentially unstable region; (b) using a dashed line to indicate the same potentially unstable region; and (c) stability circle of an unconditionally stable (different) two-port.

potentially unstable regions on a Smith chart. An alternative commonly used by RF and microwave computer-aided design programs is to use a dashed line to indicate the side of the stability circle that is potentially unstable (see Figure 2-16). Figure 2-16(a) uses shading to indicate the potentially unstable region of the Smith chart while the stability circle in Figure 2-16(b) indicates the potentially unstable region using a dashed line. The stability circle in Figure 2-16(c) identifies a two-port that is stable for all passive terminations.

If an amplifier is unconditionally stable, amplifier design is considerably simplified. Matching network design then needs to be concerned about the impact of matching networks on stability. Detailed stability analyses are presented in [11] and [12]. Note that an amplifier can be stable even if it

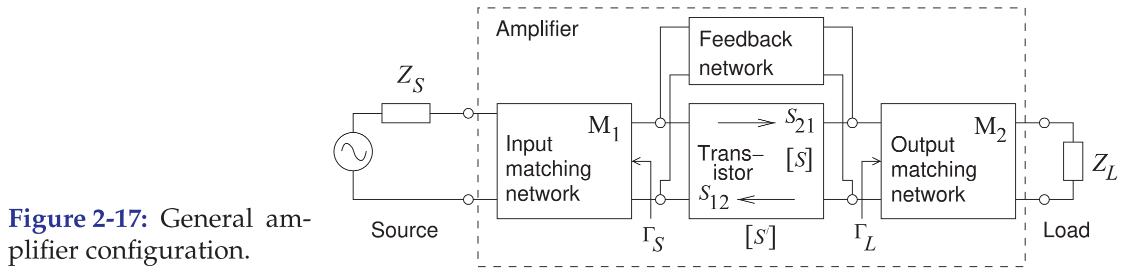


Figure 2-17: General amplifier configuration.

is not unconditionally stable.

2.6.3 Rollet's Stability Criterion — k-factor

Rollet rhymes with wallet.

The k-factor method, also known as **Rollet's stability criterion** [3, 4] is the most commonly used stability metric. It is based on the input and output reflection coefficients of an active device. The most general amplifier is depicted in Figure 2-17. Here the active device has scattering parameters

$$\mathbf{S} = [S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{2.74}$$

and, as it will be used a lot, define the determinant $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The overall amplifier has scattering parameters $\mathbf{S}'$. Γ_S is the generator reflection coefficient and Γ_L is the reflection coefficient of the load. For unconditional stability, $|S'_{11}| < 1$ and $|S'_{22}| < 1$. If $|S'_{11}| > 1$ or $|S'_{22}| > 1$, then there is a negative resistance and oscillation could possibly occur. Unconditional stability is defined as when $|S'_{11}| < 1$ for all passive loads Γ_L (i.e., $|\Gamma_L| \leq 1$) and $|S'_{22}| < 1$ for all passive source impedances Γ_S (i.e., $|\Gamma_S| \leq 1$). These inequalities are the same as saying the real part of the input and output impedances of the amplifier are positive resistances. These requirements also describe the unit circle on a Smith chart. Beginning with these definitions and ignoring the feedback network, a stability factor, k, can be defined as

$$k = \left(\frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}|\,|S_{21}|} \right), \tag{2.75}$$

where $k > 1$ is required (but not sufficient) for unconditional stability. This is the Rollet stability condition. What is done here is rolling two unconditional stability requirements (on $|S'_{11}|$ and $|S'_{22}|$) into one. If $k \leq 1$, the amplifier may not be unstable, but extra care is required when a load is presented to the amplifier. If $k > 1$, the design is relatively straightforward, but if k is near 1 or $k \leq 1$, design will be troublesome. The closer design is to the limits of operation of a device, the more likely k will be near or less than 1. For example, the limit could be the maximum stable gain at the intended frequency of operation.

It has been shown that unconditional stability is assured if

$$k = \left(\frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}|\,|S_{21}|} \right) > 1, \tag{2.76}$$

Table 2-4: Rollet's stability factor, k-factor, $|\Delta|$, and stability circle parameters of the pHEMT transistor (in Figure 2-2). For the active device to be unconditionally stable two conditions must be met: $k > 1$ and $|\Delta| < 1$. Frequencies at which the device is unconditionally stable (5–11 and 22–26 GHz) are in bold.

Freq. (GHz)	k > 1	$\|\Delta\|$ < 1	C_L	R_L	C_S	R_S
0.5	0.15178	0.62757	$1.0388 + \jmath 13.5176$	13.370	$0.92820 + \jmath 0.50682$	0.22434
1	0.24895	0.58720	$0.78679 + \jmath 7.26968$	6.9988	$0.69258 + \jmath 0.96669$	0.44107
2	0.46535	0.46821	$0.73554 + \jmath 3.96784$	3.4718	$-0.087892 + \jmath 1.481129$	0.72546
3	0.67865	0.37045	$0.63608 + \jmath 3.17780$	2.4779	$-0.86485 + \jmath 1.46382$	0.85475
4	0.91943	0.29706	$0.52381 + \jmath 2.82057$	1.9223	$-1.4232 + \jmath 1.2217$	0.91458
5	1.0838	0.24365	$0.32018 + \jmath 2.76164$	1.7276	$-1.90410 + \jmath 0.77291$	1.0132
6	1.1839	0.18765	$0.065264 + \jmath 2.679153$	1.5700	$-2.182123 + \jmath 0.024217$	1.0885
7	1.2846	0.14113	$-0.39857 + \jmath 2.97836$	1.8266	$-2.06262 - \jmath 0.85258$	1.0885
8	1.5225	0.092502	$-0.91418 + \jmath 3.21866$	2.0150	$-1.5996 - \jmath 1.4914$	0.94750
9	1.6448	0.056060	$-1.2526 + \jmath 3.0479$	1.8998	$-1.1418 - \jmath 1.8922$	0.92223
10	1.3151	0.072750	$-1.7681 + \jmath 2.6944$	2.0189	$-0.54178 - \jmath 2.13439$	1.0468
11	1.1043	0.11703	$-2.6666 + \jmath 2.4074$	2.5186	$0.24025 - \jmath 2.02042$	0.98357
12	0.98784	0.16159	$-4.4423 + \jmath 2.2978$	4.0111	$0.73109 - \jmath 1.58120$	0.74724
13	0.92131	0.18991	$-5.9502 + \jmath 1.0596$	5.1100	$0.96118 - \jmath 1.24308$	0.60117
14	0.84098	0.21905	$-5.95467 - \jmath 0.75389$	5.1368	$1.10689 - \jmath 0.97667$	0.53246
15	0.69555	0.24320	$-6.0313 - \jmath 1.9645$	5.6068	$1.20251 - \jmath 0.58617$	0.43291
16	0.63420	0.27993	$-5.7310 - \jmath 3.8333$	6.2171	$1.26271 - \jmath 0.23704$	0.39187
17	0.68792	0.32454	$-3.5163 - \jmath 5.6496$	5.9268	$1.257206 + \jmath 0.087208$	0.34232
18	0.72764	0.36197	$-1.1258 - \jmath 5.5386$	4.8824	$1.17955 + \jmath 0.29932$	0.27755
19	0.89194	0.35755	$0.72551 - \jmath 2.82689$	1.9913	$1.20751 + \jmath 0.32462$	0.27383
20	0.97085	0.32318	$1.1030 - \jmath 2.0753$	1.3671	$1.19540 + \jmath 0.46897$	0.29068
21	0.97475	0.28626	$1.3859 - \jmath 1.8451$	1.3221	$0.94075 + \jmath 0.85514$	0.27681
22	1.1014	0.28501	$2.1696 - \jmath 1.1961$	1.4187	$0.66834 + \jmath 1.07377$	0.24499
23	1.3123	0.29397	$2.35683 - \jmath 0.15064$	1.1976	$0.51539 + \jmath 1.17421$	0.22605
24	1.4714	0.28083	$2.23754 + \jmath 0.46967$	1.0569	$0.28045 + \jmath 1.30061$	0.24185
25	1.4273	0.22850	$2.2473 + \jmath 1.2506$	1.3389	$0.079906 + \jmath 1.412442$	0.31586
26	1.5308	0.17235	$2.6309 + \jmath 3.0590$	2.6671	$-0.45588 + \jmath 1.43292$	0.36774

combined with any one of the following auxiliary conditions [13–19]:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \tag{2.77}$$

$$B_2 = 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta|^2 > 0 \tag{2.78}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.79}$$

$$C_1 = 1 - |S_{11}|^2 - |S_{12}S_{21}| > 0 \tag{2.80}$$

$$C_2 = 1 - |S_{22}|^2 - |S_{12}S_{21}| > 0. \tag{2.81}$$

The conditions in Equations (2.77)–(2.81) are not independent, and it can be shown that one implies the others if $k > 1$ [13].

Rollet's stability criteria, k and $|\Delta|$, are tabulated in Table 2-4 for the pHEMT described in Figure 2-2. The device is unconditionally stable at the frequencies 5–11 GHz and 22–26 GHz. It is seen that the device could be potentially unstable at frequencies below 5 GHz and from 12 to 21 GHz. At these frequencies stability circles need to be used in designing matching networks.

Table 2-5: Edwards–Sinsky stability parameters for the pHEMT transistor documented in Figure 2-2. For stability, $\mu > 1$. The frequencies at which the device is unconditionally stable are in bold. The device is unconditionally stable at the frequencies 5–11 GHz and 22–26 GHz. The other columns refer to Equations (2.77)–(2.81) and are provided for completeness.

Freq. (GHz)	μ > 1	B_1 > 0	B_2 > 0	$\lvert\Delta\rvert$ < 1	C_1 > 0	C_2 > 0
0.5	0.18785	1.1555	0.056799	0.62757	−0.077921	0.47143
1	0.31338	1.1338	0.17657	0.58720	−0.080934	0.39770
2	0.56362	1.1086	0.45297	0.46821	0.065756	0.39356
3	0.76297	1.0884	0.63717	0.37045	0.22398	0.44958
4	0.94651	1.0631	0.76039	0.29706	0.35892	0.51029
5	1.0526	1.0434	0.83782	0.24365	0.44002	0.54284
6	1.1100	1.0341	0.89551	0.18765	0.49297	0.56225
7	1.1783	1.0703	0.88992	0.14113	0.51407	0.60424
8	1.3310	1.1120	0.87085	0.092502	0.54812	0.66871
9	1.3954	1.1104	0.88335	0.056060	0.57284	0.68634
10	1.2039	1.1068	0.88259	0.072750	0.51811	0.63023
11	1.0739	1.1550	0.81758	0.11703	0.43720	0.60592
12	0.99026	1.2715	0.67626	0.16159	0.33481	0.63244
13	0.93383	1.3461	0.58173	0.18991	0.27037	0.65257
14	0.86542	1.3788	0.52518	0.21905	0.22227	0.64910
15	0.73637	1.4578	0.42389	0.24320	0.13811	0.65507
16	0.67769	1.4752	0.36811	0.27993	0.099372	0.65290
17	0.72762	1.4461	0.34324	0.32454	0.10910	0.66053
18	0.76942	1.4300	0.30791	0.36197	0.10899	0.67006
19	0.92718	1.3348	0.40953	0.35755	0.18890	0.65152
20	0.98311	1.2924	0.49876	0.32318	0.24511	0.64191
21	0.98558	1.3331	0.50306	0.28626	0.24786	0.66286
22	1.0587	1.3627	0.47486	0.28501	0.25075	0.69466
23	1.1641	1.3295	0.49769	0.29397	0.28504	0.70093
24	1.2294	1.2872	0.55509	0.28083	0.33166	0.69771
25	1.2330	1.2866	0.60899	0.22850	0.36433	0.70313
26	1.3676	1.3398	0.60077	0.17235	0.38405	0.75358

2.6.4 Edwards–Sinsky Stability Criterion — μ-factor

Rollet's stability criterion, Equations (2.76)–(2.81), ensures unconditional stability but it does not provide a relative measure of stability. That is, the k factor cannot be used to determine how close a particular design is to the edge of stability. There is no ability to compare the relative stability of different designs. Edwards and Sinsky [13] developed a test that can be used to compare the relative stability of different designs. This is called the μ-factor stability criterion, with unconditional stability having

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} > 1. \tag{2.82}$$

An important result is that a larger value of μ indicates greater stability. The μ factor is a single quantity that provides a sufficient and necessary condition for unconditional stability. That is, it does not matter what passive source and load are presented (i.e. if $|\Gamma_S| \leq 1$ and $|\Gamma_L| \leq 1$) then the amplifier will be stable if $\mu > 1$. This contrasts with Rollet's stability criterion in which two conditions must be met.

Edwards–Sinsky stability parameters for the pHEMT transistor (documented in Figure 2-2) are shown in Table 2-5. The unconditionally stable frequencies of operation are 5–11 GHz and 22–26 GHz. These are the same unconditionally stable frequencies determined by using Rollet's stability criterion (in Table 2-4). The additional information available with the Edwards–

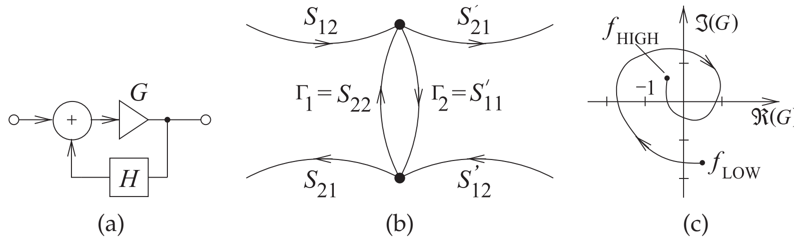


Figure 2-18: Nyquist stability analysis: (a) feedback amplifier; (b) a loop with reflection coefficients Γ_1 and Γ_2; and (c) a Nyquist stability plot of loop gain $G = -\Gamma_1\Gamma_2$ (with H set to 1).

Sinsky stability criterion is that μ indicates the relative stability. In Table 2-5, the transistor is unconditionally stable in the 5–11 GHz range, and in this range the device is most stable between 8 and 10 GHz. At the high end, above 22 GHz, the device is increasingly more stable. This can be expected to continue as the device capacitive parasitics short out the device. (The result of the low impedance of capacitors at high frequencies is that smaller RF voltages will be generated for the same drive level.) So this transistor will make a very good 8–10 GHz amplifier provided that appropriate matching networks are chosen to ensure stability below 5 GHz and above 11 GHz. Note, however, that the amplifier can be used up to about 20 GHz, but with extra care in design. Above 20 GHz the maximum unilateral transducer gain is too small to be useful (see Table 2-1, where $G_{TU,\text{max}}$ is tabulated for this transistor).

The Edwards–Sinsky stability factor, μ, is also called a **geometric stability factor**. It is the distance from the center of the Smith chart (i.e., the origin of the S parameter polar plot) to the nearest potentially unstable point on the input source plane. That is, it is the shortest distance from the origin to the input stability circle, where a negative μ indicates that the stability circle encompasses the origin of the Smith chart.

Edwards and Sinsky also defined a dual parameter, μ' [13]:

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{21}S_{12}|}. \tag{2.83}$$

This is the distance from the center of the Smith chart (i.e., the origin of the S parameter polar plot) to the nearest potentially unstable point on the output load plane. That is, it is the shortest distance from the origin to the output stability circle. If $\mu > 1$ (indicating the possibility of two-port instability), then $\mu' > 1$ as well. Thus to determine whether or not a two-port is unconditionally stable, it is only necessary to consider one of them. Also, μ and μ' are sometimes referred to as the input and output geometric stability factors respectively, and sometimes simply as μ_1 (MU1) and μ_2 (MU2), respectively. Calculating both μ and μ' is useful, as this enables the relative stability at the input and the output to be examined. Table 2-6 lists μ and μ' for the pHEMT transistor considered previously.

2.6.5 Nyquist Stability Criterion

The Nyquist stability criterion is the most complete way of analyzing stability. It is based on the analysis of the feedback system shown in Figure 2-18(a) [20–23]. The closed-loop transfer function is

$$T = \frac{G}{1 + GH}. \tag{2.84}$$

Table 2-6: Input and output Edwards–Sinsky stability parameters for the pHEMT transistor documented in Figure 2-2. For stability, $\mu > 1$ and $\mu' > 1$. The device is unconditionally stable at the frequencies 5–11 GHz and 22–26 GHz.

Freq. (GHz)	μ (MU1) (input)	μ' (MU2) (output)
0.5	0.18785	0.8332
1	0.31338	0.74811
2	0.56362	0.75828
3	0.76297	0.84547
4	0.94651	0.96112
5	1.05257	1.04174
6	1.10997	1.09373
7	1.17828	1.14339
8	1.33101	1.23947
9	1.39544	1.28779
10	1.20387	1.15528
11	1.07392	1.05108
12	0.99026	0.99479
13	0.93383	0.97018
14	0.86542	0.94371
15	0.73637	0.90486
16	0.67769	0.89289
17	0.72762	0.91790
18	0.76942	0.93939
19	0.92718	0.97655
20	0.98311	0.99342
21	0.98558	0.99451
22	1.05874	1.01979
23	1.16408	1.05629
24	1.22944	1.08865
25	1.23297	1.09884
26	1.36763	1.13596

The feedback system is unstable if the open-loop transfer function $GH = -1$. Usually in stability analysis H is considered to be 1 so that the system is unstable if the open-loop transfer function $G = -1$. Relating this to microwave circuits, every loop in a signal flow graph is considered. Generally it is sufficient to consider all possible loops containing one pair of nodes, as shown in Figure 2-18(b). It would be best to select the pair of nodes at the input or output of an active device, as the active device is surely going to be involved in instability. There is of course a chance that the critical pair of nodes will be missed, which is more likely to happen in a multistage amplifier. In that situation several pairs of nodes should be considered individually. Returning to a single pair of nodes, as shown in Figure 2-18(b), here the open-loop frequency-domain transfer function is

$$G = \Gamma_1 \Gamma_2. \tag{2.85}$$

The Nyquist stability criterion is that the system is unstable if the open-loop transfer function, G, plotted on the complex plain encircles the -1 point in a clockwise rotation with increasing frequency. The details behind this are provided in nearly every book on linear control systems (e.g. [20–23]).

To ensure stability the Nyquist plot, as Figure 2-18(c) is called, should be plotted for every loop in a system. However, experience is a good guide and only a few loops need to be considered in practice. There are also metrics such as the S probe parameter (sometimes called the G probe) used in microwave circuit simulators that provide a good estimate of whether the

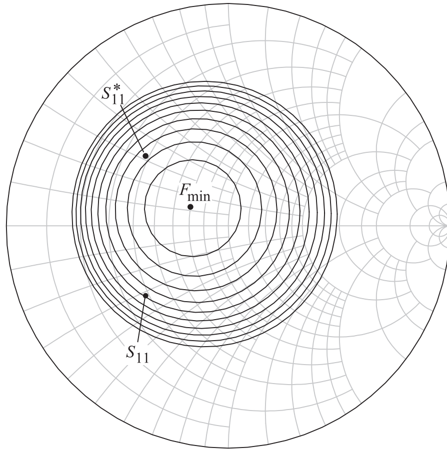


Figure 2-19: Noise figure circles at 8 GHz, plotted on the input Smith chart (i.e. on the Γ_S Smith chart) for the pHEMT transistor documented in Figure 2-2. F_{min} is 1.04 dB and the circles are in 0.1 dB circles so that the outer circle is the locus of Γ_S that will produce a noise figure of 2.04 dB.

Nyquist plot will encircle the point [24]. The utility of this is that a two-port SPROBE or GPROBE element can be inserted into a circuit and used to provide a measure of Nyquist stability by considering the open-loop gain based on reflection coefficients looking from each port.

A similar technique to applying the Nyquist stability criterion is to create a Bode plot [25]. However, this is not easy to do with many microwave circuits and not often used.

2.6.6 Summary

This section presented criteria that can be used in determining the stability of transistor amplifiers and of active devices. Stability tests should be applied to the innermost two-port, specifically the active device, to provide an enhanced confidence in design. Two criteria in the forms of FOMs were presented for unconditional stability: the k-factor and μ-factor. The k-factor, part of Rollet's unconditional stability criterion, is a test of whether a device is unconditionally stable or not. It does not provide a relative measure of stability. The μ-factor, derived by Edwards and Sinsky, is a factor that indicates the relative stability of a network. Stable amplifiers can be designed even if the amplifier is not unconditionally stable. Stability circles aid in the design of such amplifiers. Stability is an extensive topic and the reader is directed to in-depth stability analysis by Suárez and Quéré [12] for further information.

Two graphical techniques were also presented. Stability circles can be used in design to enable graphically based trade-off of stability, noise, gain, and bandwidth information displayed on a Smith chart. It is surprising how well the trade-off can be made by a designer.

2.7 Amplifier Noise

Section 4.3.6 of [26] presented a discussion of noise in amplifiers. The final result was an expression for the noise figure of an amplifier given the noise parameters of the transistor. This expression was in terms of the magnitudes of complex numbers, which, as has been seen, leads to circles when plotted on the complex plane. Thus the noise figure of an amplifier can be pictured as noise figure circles on a Smith chart. Figure 2-19 shows the noise figure

circles at 8 GHz, plotted on the input Smith chart for the pHEMT transistor documented in Figure 2-2. The center of the (almost) concentric circles is $F_{\rm min}$ and the noise figure circles show the impact of source mismatch on the noise figure. The loading conditions have little impact on the noise figure of an amplifier as long as the output matching network is lossless and the gain of the amplifier is high. These circles prove useful in making design trade-offs.

2.8 Trading Off Gain, Noise, and Stability in Amplifier Design

The design of small signal amplifiers requires a trade-off of gain, stability, and noise figure. This can be further complicated by the bandwidth requirement. So first consider the trade-offs in narrowband amplifier design with input and output matching networks and with no feedback network between the output and input of a transistor. The amplifier consists of three cascaded two-ports, one of which (the transistor two-port) can produce a potentially unstable situation. Whether the amplifier is stable or not depends on the impedance seen looking from the transistor into the output matching network and the impedance seen from the transistor looking into the input matching network. Even in narrowband amplifier design, the designer must be concerned about stability out of band. The amplifier must also be stable no matter what the values of the load or source impedances. This is because in nearly every situation there is a severe penalty if the amplifier becomes unstable and oscillates. The instrument or device in which the amplifier is embedded certainly will not work, but in the case a communication system, the entire communication system could be corrupted and system operation not restored until the offending device is tracked down and turned off.

The impedance presented to the output of the transistor is not the load impedance, it will be modified by the output matching network and by losses in cabling and filters (if any), between the output of the amplifier and the load. As far as stability is concerned, this loss helps as it reduces the range of effective loads presented to the amplifier. Ignoring loss, the amplifier load could be a short circuit, an open circuit, a match, or any combination. Thus on a Smith chart the load could be anywhere. If the output matching network is lossless and of any topology, then the impedance presented to the output of the transistor could be anywhere on the Smith chart. Now if constraints are placed on the matching network, then the region of the effective load on the Smith chart could be constrained, but this involves a more sophisticated design and is something only very experienced amplifier designers would exploit.

This discussion is designed to provide convincing evidence that the amplifier should be designed for unconditional stability. So if the load can be any value, the stability circle on the input plane defines the values of Γ_S (the reflection coefficient looking into the input matching network from the transistor) that result in unconditional stability. The matching network must be designed to provide a Γ_S that ensures stability no matter what happens to the load. Only in extreme circumstances, say at very high frequencies (where design becomes very difficult) or where there is considerable loss, say in subsequent filtering, would an experienced designer consider designing an amplifier that is not unconditionally stable. Even then design would begin with the unconditionally stable situation and morph into the potentially less

stable situation.

The stability discussion above concerns designing for stability no matter what happens to the load. The discussion is similar for designing the output matching network no matter what happens to the source. So there is an apparent flaw in the stability argument. In designing the input and output matching networks for unconditional stability, the procedure described above considers the load being corrupted on its own independent of whether the source is corrupted (e.g. by the failure of a previous stage). If something goes wrong at both the source and the load, then the amplifier could be unstable even after best efforts have been undertaken in design. It is unlikely that both the load and source would be compromised simultaneously.

Now consider the trade-off between gain and the noise figure. This could be a difficult trade-off, but a simple design procedure has been adopted. If the amplifier is the first stage in a cascade of amplifiers, then the preferred choice is that the emphasis for the first stage is to design it for the minimum noise figure and ensure that at least some gain is obtained. In subsequent stages the emphasis is on gain and the noise figure is given little consideration. This trade-off is based on Friis's formula for the noise figure of cascaded systems, which indicates that if the gain of the first stage is high, then the noise figure of the first stage dominates the system noise figure. A better overall trade-off can be achieved using the optimizer provided in a microwave design tool. However, the manually directed design must be done first or the optimization problem is too difficult.

With wideband designs of a half-octave bandwidth amplifier, the additional problem of achieving stability and the minimum noise figure, or stability and maximum gain, over the frequency band is a further complicating factor. Here the inventive aspect of design is developing a matching network that has the desired frequency response.

Further complicating this is that efficiency and distortion must be considered as well. Even with a small signal, distortion is a concern, as a design goal is minimizing DC power consumed. This is because reducing distortion usually results in increased DC power consumption.

2.9 Case Study: Narrowband Linear Amplifier Design

The design procedure for linear amplifiers is well developed and the strategy forms the basis for all amplifier design. An amplifier has three major components: an input matching network, an active device, and an output matching network (see Figure 2-20). There are a number of design choices to be made and these will be illustrated by considering the design of an amplifier for maximum gain using the discrete pHEMT transistor examined previously (see Figure 2-2). The design specifications are

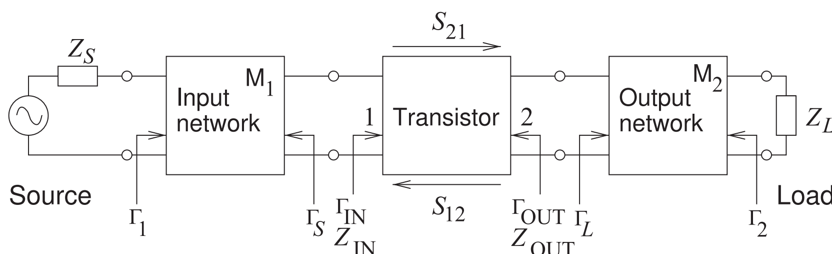
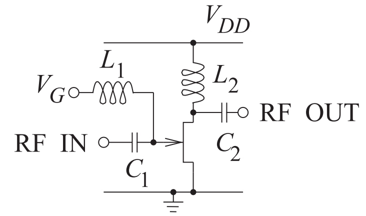


Figure 2-20: Linear amplifier comprising input and output matching networks and an active device in a specific configuration forming a two-port.

Figure 2-21: Bias configuration for pHEMT amplifier. L_1 and L_2 are RF chokes and large enough to block RF. C_1 and C_2 are DC blocking capacitors that block DC but allow RF to pass with negligible impedance.



Gain:	maximum gain at 8 GHz
Topology:	three two-ports (input and output matching networks, and the active device)
Stability:	broadband stability
Bandwidth:	maximum that can be achieved using two-element matching networks
Source impedance:	$Z_S = 50\ \Omega$
Load impedance:	$Z_L = 50\ \Omega$

2.9.1 Bias Circuit Topology

The first design step is to choose a biasing configuration, and this is directly related to the output voltage swing supported. The inductively biased configuration in Figure 2-21 will be used. Here L_1 and L_2 are RF chokes and large enough to block RF. C_1 and C_2 are DC blocking capacitors that block DC but allow RF to pass with negligible impedance. The input matching network is attached to the RF IN terminal and the output matching network is attached to the RF OUT terminal. V_{DD} is the supply voltage and V_G is the DC gate voltage typically provided by an analog integrated circuit available in conjunction with most RF designs. An additional design objective is to absorb the biasing circuit into the matching networks.

2.9.2 Stability Considerations

It is not sufficient to consider a single frequency in design, as stability must be ensured at low and high frequencies. The stability factor of the active device was given in Table 2-5. This indicates that the device is unconditionally stable from 5 to 11 GHz and from 22 to 26 GHz. At the high-frequency end, the gain of the device reduces rapidly with increasing frequency as the capacitive parasitics begin dominating transmission through the device. Therefore it is reasonable to assume that the device is unconditionally stable above 22 GHz.

Design nearly always commences with the output matching network. The first design step is to choose a matching network that will provide the appropriate impedances to ensure stability below 5 GHz and above 11 GHz. To do this the stability circles must be considered, as the device is only conditionally stable at these frequencies. The center and radius of the input and output stability circles are listed in Table 2-4. These are plotted in Figure 2-22 for selected frequencies.

2.9.3 Output Matching Network Design

The output stability circle at 1 GHz (see Figure 2-22(a)) indicates that for stable, low-frequency amplification, the output matching network, as seen from the transistor, could look like a short circuit, a matched load, or a capacitor at low frequencies. Figure 2-22(c), the output stability circle at

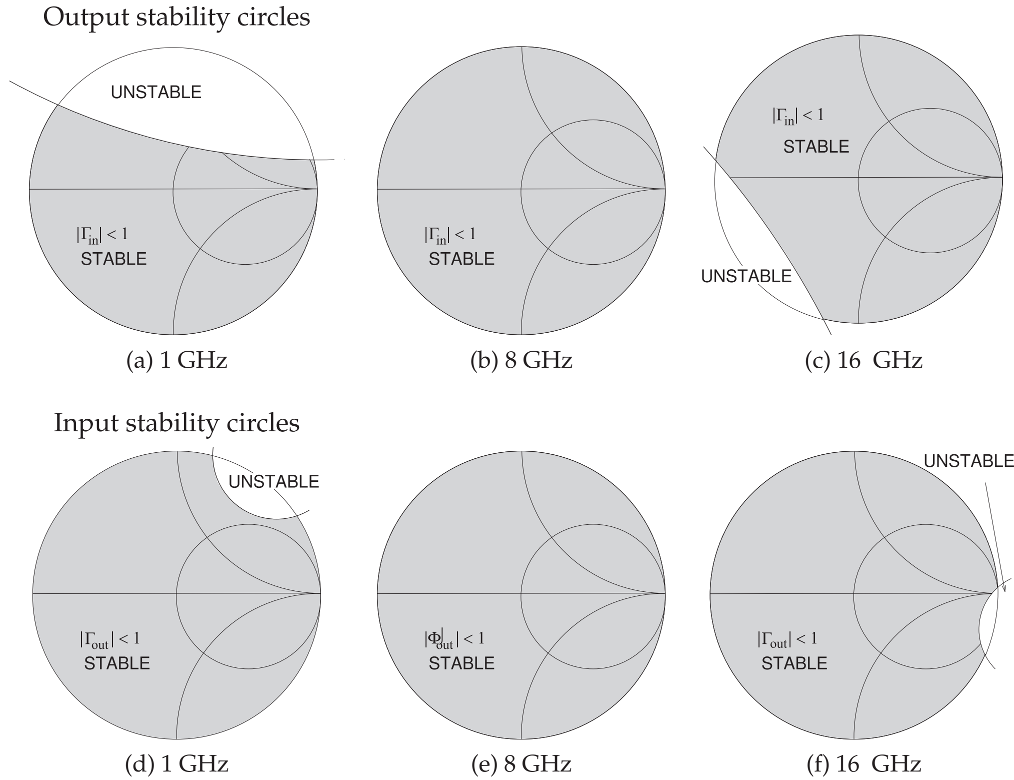


Figure 2-22: Input and output stability circles on the complex reflection coefficient planes for $|S_{11}| < 1$ and $|S_{22}| < 1$.

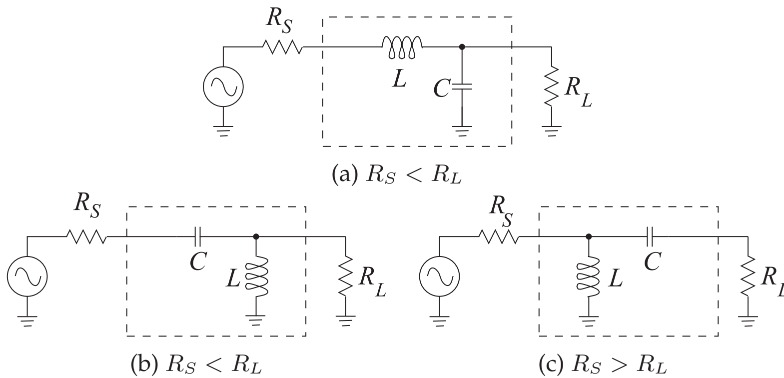


Figure 2-23: Output matching network candidates required for out-of-band stability. The active device is on the left.

16 GHz, indicates that for stable, high-frequency amplification the output matching network, as seen from the transistor, could look like an open circuit or a matched load at high frequencies. As expected, the output stability circle at 8 GHz (see Figure 2-22(b)) indicates unconditional stability. Examining the two-element matching networks in Figure 6-7 of [2], there are three candidate output matching networks that are shown in Figure 2-23.

From Figure 2-2, the device S parameters at 8 GHz are as follows:

$$S_{11} = 0.486\angle 140.4^\circ \qquad S_{21} = 3.784\angle 11.2^\circ$$
$$S_{12} = 0.057\angle 6.4^\circ \qquad S_{22} = 0.340\angle{-99.1}^\circ.$$

To start, ignore S_{12} so that $\Gamma_{\rm OUT} = S_{22} = 0.340\angle{-99.1}$. There is little choice here as $\Gamma_{\rm OUT}$ depends on the input matching network that has not yet been designed. It would have been possible to begin with the input matching network and make this approximation for $\Gamma_{\rm IN}$. However, experience is that the error introduced by starting with the output matching network is less. Once the output matching network has been designed, $\Gamma_{\rm IN}$ can be calculated without approximation. A thorough design would complete the first pass of the design and then make one more pass without the approximation that ignores S_{12}. Now, with $\Gamma_{\rm OUT} = S_{22}$, the output impedance of the active device is

$$\begin{aligned} Z_{\rm OUT} &= Z_0 \frac{1+\Gamma_{\rm OUT}}{1-\Gamma_{\rm OUT}} = Z_0 \frac{1+S_{22}}{1-S_{22}} \\ &= (50\ \Omega)\frac{1+(0.340\angle-99.1^\circ)}{1-(0.340\angle-99.1^\circ)} = (50\ \Omega)\frac{1+(-0.053774-\jmath 0.335721)}{1-(-0.053774-\jmath 0.335721)} \\ &= 36.153 - \jmath 27.447\ \Omega, \end{aligned} \tag{2.86}$$

or $Y_{\rm OUT} = 1/Z_{\rm OUT} = 0.017547 + \jmath 0.013322\,{\rm S}$. The output of the active device looks like a 56.99 Ω resistor in parallel with a capacitor with a reactance of $-75.064\,\Omega$. So taking into account the bias objectives and the available output matching networks in Figure 2-23, the matching network topology of Figure 2-23(c) will be used where the source in the matching network is the active device. So the output matching network problem is as shown in Figure 2-24. This choice enables the inductor to be used to apply bias.

The complete output matching problem is shown in Figure 2-24(a). In part, the parallel configuration of the active device output impedance was chosen, as this is closer to reality since there is a capacitance at the output of the transistor. Resonance, as shown in Figure 2-24(b), will be used to cancel the effect of the active device capacitance, so that the matching problem reduces to that shown in Figure 2-24(c). Using the procedure outlined in Section 6.4.2 of [2],

$$|Q_S| = |Q_P| = \sqrt{\frac{R_S}{R_L} - 1} = \sqrt{\frac{56.99}{50} - 1} = 0.3739 \tag{2.87}$$

$$Q_S = \left|\frac{X_S}{R_L}\right| = \left|\frac{X_S}{50\ \Omega}\right| = 0.3739 \text{ and } Q_P = \left|\frac{R_S}{X_P}\right| = \left|\frac{56.99\ \Omega}{X_P}\right| = 0.3739, \tag{2.88}$$

$$\text{so } X_S = -18.70\,\Omega \quad \text{and} \quad X_P = 152.4\,\Omega. \tag{2.89}$$

Now $X_x = -75.064\ \Omega$, so $75.064\ \Omega$ must be added to X_P in parallel, and the reactance of L_o is $50.29\ \Omega$, thus (at 8 GHz)

$$L_o = 1.00\,{\rm nH} \quad \text{and} \quad C_o = 1.064\,{\rm pF}. \tag{2.90}$$

The final output matching network design is shown in Figure 2-24(d).

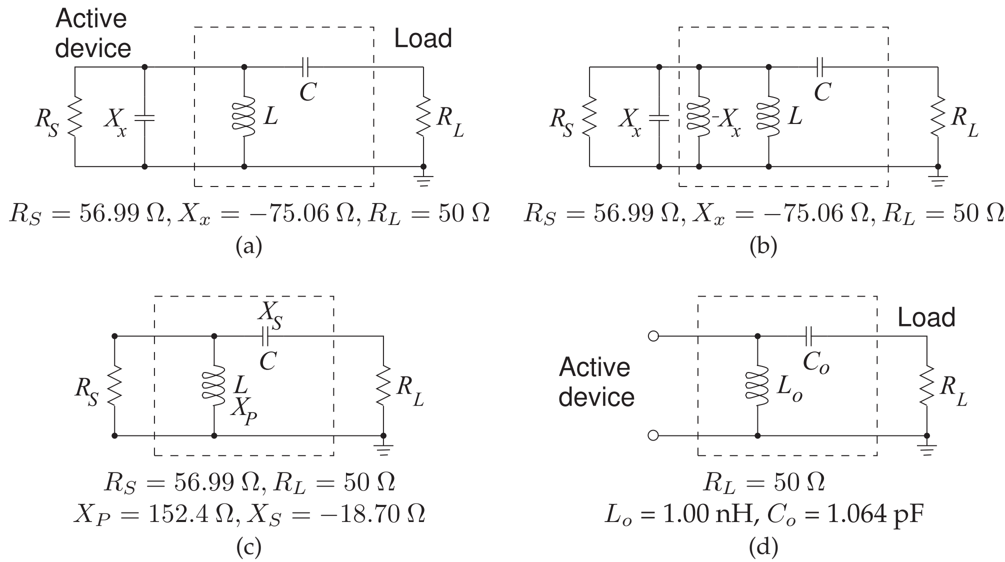


Figure 2-24: Steps in the design of the output matching network: (a) active device presents itself as a resistance in parallel with a capacitive reactance to the output matching network; (b) with inductor to resonate out active device reactance; (c) simplified matching network problem; and (d) final output matching network design.

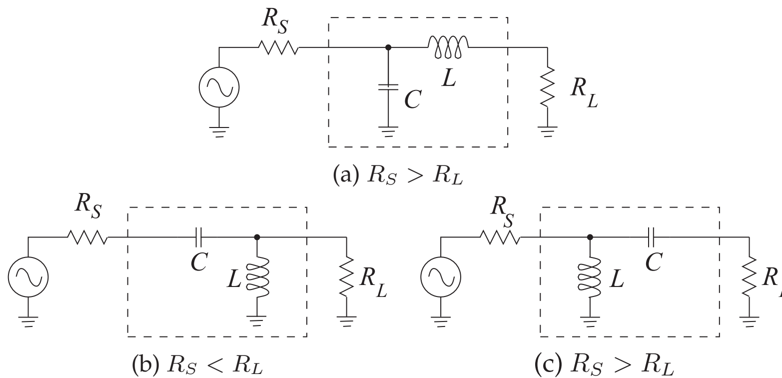


Figure 2-25: Input matching network candidates required for out-of-band stability. The active device is on the right.)

2.9.4 Input Matching Network Design

The input stability circle at 1 GHz (Figure 2-22(d)) indicates that at 1 GHz, the input matching network, as seen from the transistor, could look like a short circuit, a matched load, or a capacitor at low frequencies. Figure 2-22(f), the input stability circle at 16 GHz, indicates that the input matching network, as seen from the transistor, could look like a short circuit or a matched load at high frequencies. Examining the two-element matching networks in Figure 6-7 of [2], there are three candidate input matching networks as shown in Figure 2-25.

The reflection coefficient looking into the output matching network from the active device is $\Gamma_L = S_{22}^* = 0.340\angle 99.1°$ because of the design decision to ignore S_{12} for the output matching network. Now that the output matching

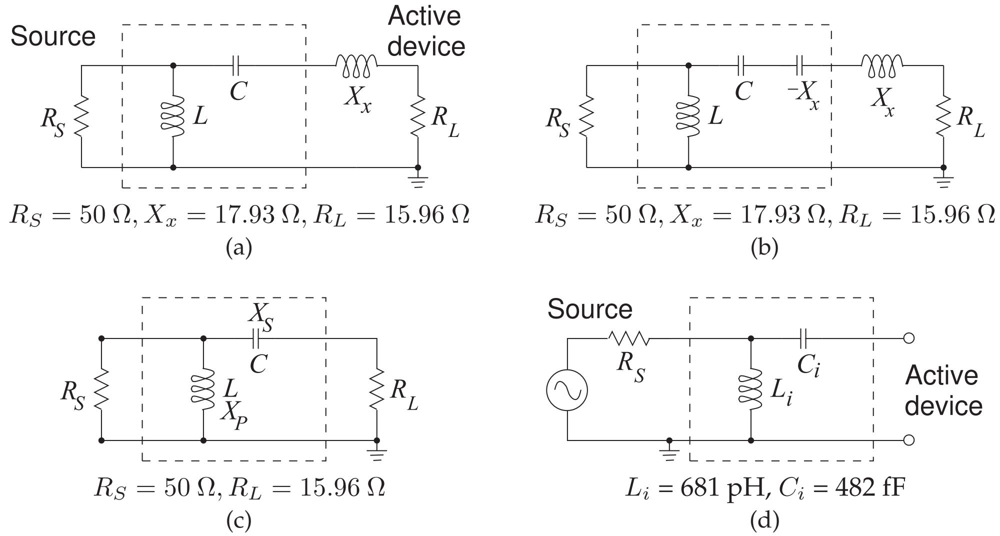


Figure 2-26: Steps in the design of the input matching network: (a) active device presents itself as a resistance in series with an inductive reactance to the input matching network; (b) with a capacitor to resonate out the active device reactance; (c) simplified matching network problem; and (d) final output matching network design.

network has been designed, the feedback parameter need no longer be ignored. So

$$\Gamma_{\text{IN}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.91}$$

$$= (0.486\angle 140.4°) + \frac{(0.057\angle 6.4°)(3.784\angle 11.2°)(0.340\angle 99.1°)}{1 - (0.340\angle{-99.1°})(0.340\angle 99.1°)} \tag{2.92}$$

$$= -0.4117 + \jmath 0.3839. \tag{2.93}$$

That is, $Z_{\text{IN}} = 15.959 + \jmath 17.935\ \Omega$. So taking into account the bias objectives and the output matching networks shown in Figure 2-25, the matching network topology of Figure 2-25(c) will be used (where the load is the active device). The input matching network problem is as shown in Figure 2-26(c). (Biasing cannot be incorporated into this matching network.) Now

$$|Q_S| = |Q_P| = \sqrt{\frac{R_S}{R_L} - 1} = \sqrt{\frac{50}{15.959} - 1} = 1.4605 \tag{2.94}$$

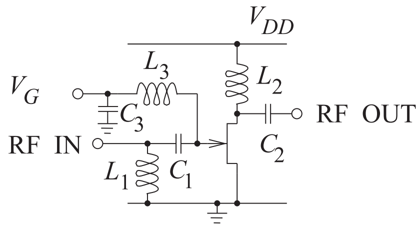
$$Q_S = \left|\frac{X_S}{R_L}\right| = \left|\frac{X_S}{15.959\ \Omega}\right| = 1.4605 \quad \text{and} \quad Q_P = \left|\frac{R_S}{X_P}\right| = \left|\frac{50\ \Omega}{X_P}\right| = 1.4605. \tag{2.95}$$

$$\text{So} \qquad X_S = -23.31\ \Omega \quad \text{and} \quad X_P = 34.23\ \Omega. \tag{2.96}$$

Since $X_x = 17.935\ \Omega$, $-17.935\ \Omega$ must be added to X_S, and the reactance of C_i is 41.24 Ω, thus (at 8 GHz),

$$L_i = 681\ \text{pH} \quad \text{and} \quad C_i = 482\ \text{fF}. \tag{2.97}$$

The final input matching network design is shown in Figure 2-24(d).



$L_1 = L_i = 681$ pH
$L_2 = L_o = 1.00$ nH
$L_3 = 10$ nH
$C_1 = C_i = 482$ fF
$C_2 = C_o = 1.064$ pF
$C_3 = 100$ pF

Figure 2-27: Final amplifier schematic.

2.9.5 Bias Network Design

The final schematic of the linear amplifier design is shown in Figure 2-27. The output matching network, L_2 and C_2, enabled the biasing inductor to be replaced by L_2. So the output bias circuitry is absorbed into the output matching network. A similar result is not obtained with the input matching network, L_1 and C_1. A separate gate bias network is still required. L_3 should be a large enough value for it to act as an RF choke. A value of 10 nH provides a reactance of approximately 500 Ω at 8 GHz. The value of C_3 = 100 pF is chosen large enough to provide an RF short and stabilize the DC bias, V_G. This is a surprisingly simple circuit that provides maximum gain at 8 GHz, ensures out-of-band stability, and provides DC bias. Another design iteration with a more sophisticated input matching network may enable the separate bias inductor L_3 to be eliminated. As it is, the gate bias circuit further ensures stability at low frequencies, as then the gate tends to be shorted out. The amplifier has a calculated transducer gain of 13.2 dB, which can be compared to the gains reported in Table 2-2, where gain metrics were determined with S_{12} ignored.

Linear amplifier design for a specific gain is also possible. Now the errors involved in ignoring S_{12} during the design process are significant and a full bilateral treatment is required. This design approach is described in references [11, 27, 28].

2.10 Summary

This chapter addressed the design of narrowband amplifiers, but this forms the basis of wideband and power amplifier design to be considered in the following chapters. The bandwidth of an amplifier is dictated by the frequency-dependent characteristics of the active device and at microwave frequencies the device parasitic capacitances are usually significant. Without special broadbanding concepts, the narrowband approach covered in this chapter is good, usually, for amplifier designs with up to 5% bandwidth.

The basic topology used in amplifiers is an input matching network, an active device, and an output matching network. This arrangement is one of three cascaded two-ports. Sometimes an additional two-port is used in parallel with the active device to provide feedback and ensure stability or a flat gain response over frequency. With narrowband design the use of a feedback network is rarely required. The input matching network provides near-maximum power transfer from the system impedance to the usually higher input impedance of the active device. The near-maximum qualification is used since the requirements for maximum power transfer at the input conflict with the conditions for best noise performance. This originates because the active device has multiple partially correlated

physical noise sources and the input matching network affects how the correlated noise sources are combined so that it is possible to minimize their contributions. The active device is followed by an output matching network that matches the output impedance of the active device to the usually higher system impedance. In narrowband amplifier design the device capacitive parasitics are often incorporated into the matching networks. The topology of the input and output matching networks is chosen to ensure out-of-band stability and provide bias with minimum additional components.

Amplifier design is driven by metrics for the power gains at various optimum conditions, and the various gain metrics are used at various stages in design. The gain metrics are also used in choosing an active device and in estimating the design complexity that can be expected.

Amplifier design is a major endeavor and many books have been written about particular aspects of RF and microwave amplifier design. This chapter covered the main topics and also presented treatments that are broadly applied. The reader is directed to references [11, 14, 29–36] for specialized aspects of amplifier design. Numerous references are available for understanding, analyzing, and characterizing distortion in greater depth than covered here [37–48].

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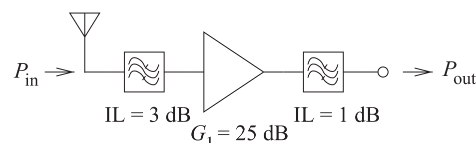
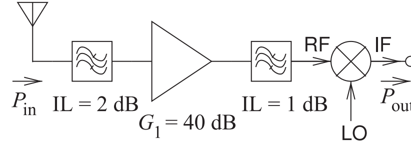
2.12 Exercises

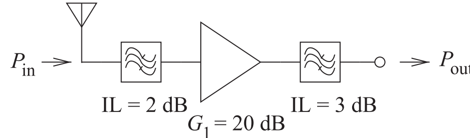
1. What is the gain of the following receiver system?



2. In the system below the mixer has a conversion loss of 10 dB. What is the gain of the receiver system?



3. What is the gain of the receiver system below?



4. A source that drives an amplifier has an available output power of 1 mW. The amplifier has been optimally matched in a 50 Ω system and then has a small signal gain of 20 dB. The amplifier load is now changed and the new load is mismatched with a VSWR of 1.5. What is the power delivered to the new load?

5. A MOSFET amplifier has the small signal S parameters $S_{11} = 0.3\angle 85°$, $S_{12} = 0.05\angle 15°$, $S_{21} = 2.5\angle 100°$, and $S_{22} = 0.85\angle -50°$ at 5.6 GHz.
   1. What is the maximum unilateral transducer gain?
   2. What is the maximum available power gain?
   3. What is the maximum stable power gain?
   4. What is the unilateral power gain?

6. An amplifier has a gain of 10 dB, an output power of 1 W, and a power-added efficiency of 25%.
   (a) What is the total efficiency of the amplifier as a percentage?
   (b) What is the efficiency of the amplifier as a percentage?

7. A Class A BJT amplifier has a collector bias voltage of 5 V and a collector bias current of 100 mA.
   (a) What is the efficiency of the amplifier if the RF output power is 1 mW?
   (b) What is the efficiency of the amplifier if the RF output power is 10 mW?
   (c) What is the efficiency of the amplifier if the RF output power is 100 mW?

8. A Class A MOS RF amplifier has a drain bias voltage of 20 V and a drain bias current of 1 A. If the output power of the amplifier is 5 W and the available input power is 1 W, what is the power-added efficiency of the amplifier?

9. A power amplifier with a gain of 10 dB draws 100 W of DC power and delivers 50 W of RF output power. What is the power-added efficiency of the amplifier?

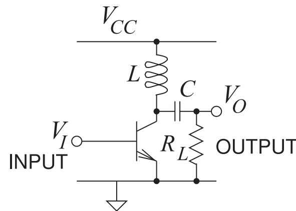
10. A FET power amplifier with a gain of 10 dB draws 100 W of DC power and delivers 50 W of RF output power. What is the drain efficiency of the amplifier?

11. Consider the design of a 15 GHz inductively biased Class A amplifier using a transistor with 50 Ω S parameters $S_{11} = 0.5\angle 45°$, $S_{12} = 0.1\angle 0\circ$, $S_{21} = 2\angle 90°$, and $S_{22} = 0.75\angle 45°$.
   (a) If the input of the transistor is terminated in 50 Ω, what is the impedance looking into the output of the transistor?
   (b) Design a two-element lumped-element output matching network for maximum power transfer from the output of the transistor into a 50 Ω load.

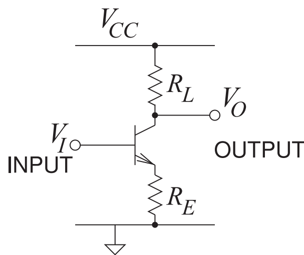
12. Consider the design of a 15 GHz inductively biased Class A amplifier using a transistor with 50 Ω S parameters $S_{11} = 0.96\angle 85°$, $S_{12} = 0.056\angle 15°$, $S_{21} = 2.56\angle 100°$, and $S_{22} = 0.320\angle 54.6°$.
   (a) If the input of the transistor is terminated in 50 Ω, what is the impedance looking into the output of the transistor?
   (b) Design a two-element lumped-element output matching network for maximum power transfer from the output of the transistor into a 50 Ω load.
   (c) As the first step in evaluating the power gain of the amplifier, determine which of the various gains defined for an amplifier is the power gain here. That is, several gains are defined in terms of S parameters and reflection coefficients (e.g., available gain, maximum stable gain, etc.). Which of these can be used to evaluate the power gain in this circumstance where there is not an input matching network, but there is an output matching network?
   (d) What is the power gain of the amplifier in decibels?

13. Consider the design of a 10 GHz inductively biased Class A amplifier using a transistor with 50 Ω S parameters $S_{11} = 0.9\angle 80°$, $S_{12} = 0.06\angle 15°$, $S_{21} = 2.5\angle 10°$, and $S_{22} = 0.3\angle 45°$.
   (a) If the input of the transistor is terminated in 55.5 Ω, what is the impedance looking into the output of the transistor?
   (b) Design a two-element lumped-element output matching network for maximum power transfer from the output of the transistor into a 50 Ω load.
   (c) What is the power gain of the amplifier in decibels?

14. The Class A BJT amplifier in the figure below has an RF choke providing collector current and acts as an open circuit at RF. The load, R_L, is driven through a capacitor, C, which is effectively a short circuit at RF. The maximum undistorted efficiency of this circuit is 50%. Derive this efficiency. Ignore the base-emitter voltage drop, $V_{CE,\min}$, and note that the maximum of V_O is $2V_{CC}$, allowing a voltage swing of $\pm V_{CC}$ around the collector quiescent operating voltage. [Parallels Example 2.2]



15. The Class A BJT amplifier in the figure below has a load, R_L, and a maximum undistorted efficiency of 25%. Derive the efficiency of this amplifier in terms of R_E and R_L. Assume that V_{CC} is much greater than V_{BE}. [Parallels Example 2.2]



16. Consider a Class C BJT amplifier with a resistive bias that is also the RF load. The supply voltage is 10 V.
    (a) Draw the loadline of the amplifier and indicate the loadline and bias point.
    (b) What is the collector bias current with no RF input signal?
    (c) With the RF input to the amplifier having a power of 10 mW, the RF output power is 100 mW, the quiescent collector-emitter voltage is 6 V, and the quiescent collector current is 20 mA. What is the power-added efficiency of the amplifier under these conditions?

17. Consider the design of a 15 GHz inductively biased Class A amplifier using the transistor in Figure 2-2 and with a 50 Ω source.
    1. What is the impedance presented at the output of the transistor?
    2. Design a two-element output matching network for maximum power transfer into a 50 Ω load.

18. A MOSFET amplifier has the small signal S parameters $S_{11} = 0.8\angle 90°$, $S_{12} = 0.05\angle 0°$, $S_{21} = 2.5\angle 0°$, and $S_{22} = 0.8\angle 0°$ at 5.6 GHz.
    (a) Calculate the radius and center of the input stability circle.
    (b) Draw conclusions from the plot of the input stability circle. That is, what restrictions are placed on the input matching network if the amplifier load is passive?

19. A MOSFET amplifier has the small signal S parameters $S_{11} = 0.9\angle 85°$, $S_{12} = 0.05\angle 15°$, $S_{21} = 2.5\angle 100°$, and $S_{22} = 0.85\angle -50°$ at 5.6 GHz.
    (a) Calculate the radius and center of the output stability circle.
    (b) Draw the output stability circle on a Smith chart.
    (c) Draw conclusions from the plot of the output stability circle. That is, what restrictions are placed on the output matching network?

20. A MOSFET amplifier has the small signal S parameters $S_{11} = 0.9\angle 85°$, $S_{12} = 0.025\angle 15°$, $S_{21} = 3\angle 100°$, and $S_{22} = 0.85\angle -50°$ at 2 GHz.
    (a) Calculate the radius and center of the input stability circle.
    (b) Draw conclusions from the plot of the input stability circle. That is, what restrictions are placed on the input matching network?

21. A MOSFET amplifier has the small signal S parameters $S_{11} = 0.9\angle 85°$, $S_{12} = 0.05\angle 15°$, $S_{21} = 2.5\angle 100°$, and $S_{22} = 0.85\angle - 50°$ at 5.6 GHz.
    (a) What is the k-factor of Rollet's stability criterion?
    (b) What does the k-factor indicate about the stability of the transistor?
    (c) What is the μ-factor of the Edwards–Sinsky stability criterion?
    (d) What does the Edwards–Sinsky stability criterion indicate about the stability of the transistor?

22. Consider the design of a 15 GHz inductively biased Class A amplifier using the pHEMT transistor documented in Figure 2-2. Use the topology shown in Figure 2-20.
    (a) If the input of the transistor is terminated in 55.5 Ω, what is the impedance looking into the output of the transistor?
    (b) Design a two-element output matching network for maximum power transfer into a 50 Ω load.

23. Consider the design of a 15 GHz inductively biased Class A amplifier using the pHEMT transistor documented in Figure 2-2. Use the topology shown in Figure 2-20.
    (a) If the input of the transistor is terminated in 150 Ω, what is the impedance looking into the output of the transistor?
    (b) Design a two-element output matching network for maximum power transfer into a 50 Ω load.
24. Consider the design of a 15 GHz inductively biased Class A amplifier using the pHEMT transistor documented in Figure 2-2. Use the topology shown in Figure 2-20.
    1. If the input of the transistor is terminated in 200 Ω, what is the impedance looking into the output of the transistor?
    2. Design a two-element output matching network for maximum power transfer into a 50 Ω load.
25. Design an amplifier for maximum stable gain using the discrete pHEMT transistor described in Figure 2-2. The design specifications are

Gain:	maximum gain at 24 GHz
Topology:	three two-ports (input and output matching networks, and the active device)
Stability:	broadband stability
Bandwidth:	maximum that can be achieved using two-element matching networks
Source Z:	$Z_S = 10\ \Omega$
Load Z:	$Z_L = 50\ \Omega$

26. Design an amplifier for maximum stable gain using the discrete pHEMT transistor described in Figure 2-2. The design specifications are

Gain:	maximum gain at 23 GHz
Topology:	three two-ports (input and output matching networks, and the active device)
Stability:	broadband stability
Bandwidth:	maximum that can be achieved using two-element matching networks
Source Z:	$Z_S = 50\ \Omega$
Load Z:	$Z_L = 50\ \Omega$

27. An inductively biased Class A HBT amplifier is biased with a collector-emitter quiescent voltage of 5 V and a quiescent collector-emitter current of 100 mA. When operated at the 1 dB gain compression point, the input RF power is 10 mW and the output power is 100 mW. Consider that the RF signal is a sinewave, and note that the quiescent collector-emitter voltage will be the supply rail voltage.
    (a) What is the quiescent DC power consumed? Express your answer in milliwatts.
    (b) What is the output power in dBm?
    (c) What is the efficiency of the amplifier? Note that the efficiency of a Class A amplifier can be more than 25% if distortion is tolerated.
    (d) What is the power-added efficiency of the amplifier?
    (e) If the input power is reduced by 10 dB so that the amplifier is no longer in compression, will the DC quiescent point change? Explain your answer.
    (f) If the input power is reduced 10 dB so that the amplifier is no longer in compression, what is the output power in dBm? Ignore any change in the quiescent point.
    (g) With 1 mW input power, what is the power-added efficiency of the amplifier if the quiescent point does not change?

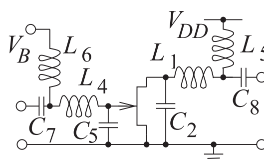
2.12.1 Exercises By Section

†challenging, ‡very challenging

§2.1 1, 2, 3
§2.3 4, 5†
§2.4 6, 7, 8, 9, 10
§2.5 11†, 12†, 13†, 14†, 15†, 16†, 17
§2.6 18†, 19†, 20, 21
§2.9 22†, 23†, 24†, 25‡, 26‡, 27†

2.12.2 Answers to Selected Exercises

1 1 dB
6 27.8%
5(d) 14.2 dB
10 50%
11(a) $436 - \jmath 105.6\ \Omega$
12(a) $61.3 - \jmath 35.6\ \Omega$
21(c) 0.563
25



$L_1 = 36.8$ fH, $C_2 = 36.8$ fF
$L_3 = 321$ pH, $C_4 = 27.4$ fF
L_5, L_6, C_7, C_8 are large
27 2.3

CHAPTER 3

Wideband Amplifiers

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3.1 Introduction

Wideband amplifier design requires the synthesis of matching networks that provide a match over considerable bandwidths. The divisions between narrowband, wideband and ultra-wideband microwave amplifier design depend on operating frequency and the amplifier efficiency required. Generally, however, a microwave amplifier with a half-octave bandwidth, e.g. 2 to 3 GHz, is regarded as a wideband design.

The essential amplifier design problem is that at microwave frequencies the parasitic input and output capacitances of a transistor are significant and these must be canceled to achieve maximum power transfer. Synthesis of the input and output matching networks of a microwave amplifier at a single frequency leads to a narrowband amplifier with a bandwidth of perhaps 2–3%. At lower frequencies where the parasitic capacitances are less significant, the fractional bandwidth may be greater. An ideal response would be achieved if there were negative capacitors and typically resonance of lumped-elements can be used to at least partially present a negative capacitance-like characteristic over about a quarter-octave bandwidth.

The dominant reactive parasitics of a transistor are its input and output capacitances, but also the feedback capacitor between the collector/drain and base/gate becomes important at higher frequencies. Ignoring the feedback capacitance and thinking just about the input of the transistor, the input of the transistor is a capacitance sometimes in series (for a BJT)

and sometimes in parallel (for a FET) with the resistance describing the absorption of RF input power by the transistor. Ideal matching requires the synthesis of a negative capacitor (i.e., an element which has an inductive reactance that reduces with frequency). Simply using an inductor to provide matching provides a matching element whose impedance increases with frequency. The wideband input matching problem becomes essentially the synthesis of a terminated two-port network with an input impedance that has the required negative capacitance characteristic. This is not easy to achieve using lumped-elements alone.

This chapter presents three strategies for designing wideband linear amplifiers. One uses the image impedance method in which the required negative capacitance impedance is realized using a transmission line network. The next is a multistage distributed amplifier that incorporates the transistor capacitances into a transmission line. The third approach is akin to a parallel coupled-line filter design.

3.1.1 Wideband Amplifier Design Strategies

Generally a wideband amplifier has a half-octave bandwidth, e.g. 8 GHz to 12 GHz. Multiple objectives must be met in wideband amplifier design. Of course the gain must be flat over the specified bandwidth but it is also important to meet noise and stability objectives over the bandwidth. Of course the amplifier must be stable out-of-band as well. It is generally not possible to meet all of these objectives using computer optimization and it is necessary to simplify the design process. When computer optimization is used, it is done in stages and begins with a prototype design that is not too far away from the final design.

An ultra-wideband amplifier has a bandwidth of more than a half octave. There are two approaches to achieving ultra-wide bandwidth and both types of amplifiers have low efficiency. The first category of ultra-wideband amplifier is the distributed amplifiers which achieves multi-octave bandwidth by incorporating the parasitic capacitances of transistors in an artificial transmission line. The parasitic inductances are usually negligible but if not, they are incorporated in the artificial transmission line. In effect there is a multi-stage amplifier and each stage must be a Class A stage and thus have very low efficiency, think 5%. Ultra-wideband distributed amplifiers tend to be used in instrumentation. A non-aggressive Class A amplifier design is more likely to be stable. Distributed amplifier design is considered in Section 3.2 and a case study of a distributed amplifier in Section 3.3.

A second type of ultra-wideband amplifier is an operational amplifier with very high levels of feedback. In an operational amplifier the open loop amplifier (without feedback) has very high gain, but a gain that varies significantly with frequency. Then feedback is used, the loop is closed, to effectively throw away most of the gain to obtain an overall flatter gain over a wide bandwidth. This type of amplifier has very low efficiency and usually the gains available from microwave transistors are not high enough anyway. Even with the highest performing transistors, that is ones with very high S_{21} to S_{12} ratio, the transistors tend to be very expensive requiring finer lithography to achieve the required shorter gate. Microwave operational amplifiers really are not viable and so will not be considered further.

The highest bandwidth of a microwave amplifier that achieves flat gain across the band, has good efficiency, and meets noise and stability requirements is about half an octave. A straight-forward approach would seem to be to simultaneously design the input and output networks and employ computer optimization. This is complicated at microwave frequencies because feedback from the output to the input, i.e. S_{12}, is large. Design then becomes an optimization problem with multiple objectives and many parameters to adjust. An optimization-only approach rarely works. It is essential to simplify the problem and approach design in stages. The most successful wideband amplifier design technique is the negative image design method which begins by placing hypothetical negative capacitors in parallel with the input and output capacitances of a transistor. The procedure will be described in Section 3.4 and then a case study is presented in Section 3.5.

A final class of microwave amplifiers that achieves reasonably high bandwidths are the differential amplifiers used in RFICs. These are considered in Sections 3.6–3.8.

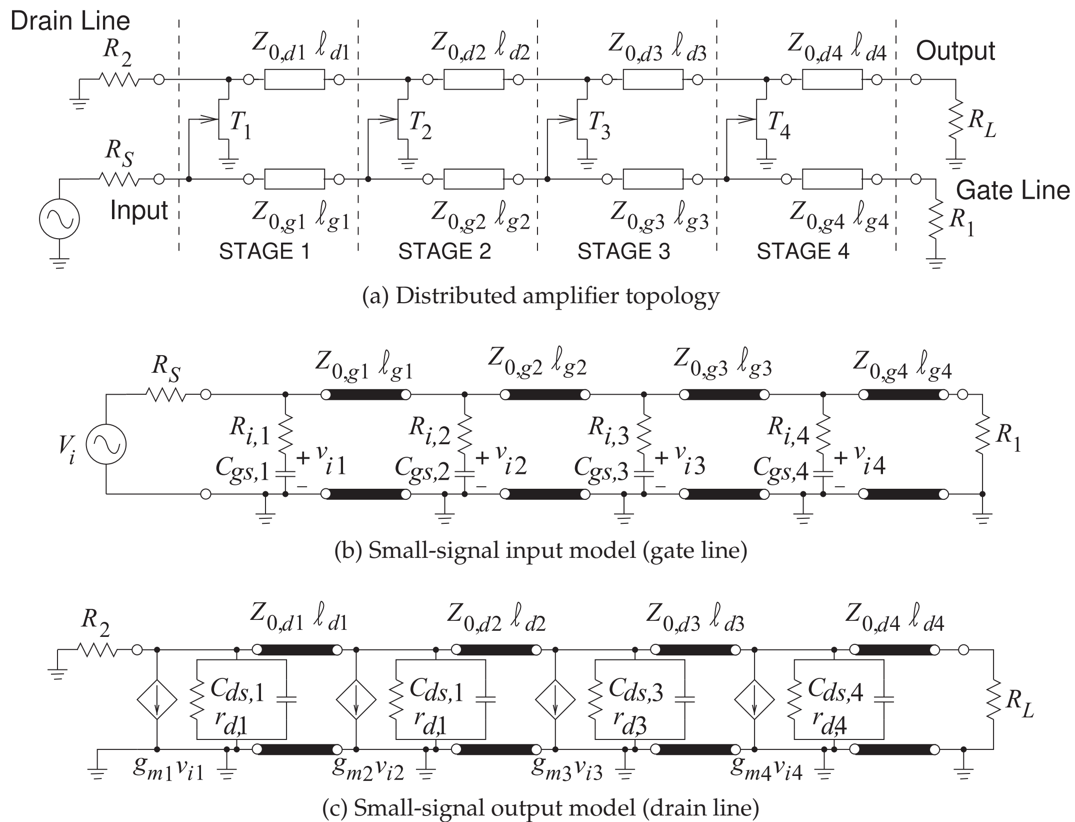
3.2 Distributed Amplifiers

Distributed amplifiers use the ability of transmission lines to combine the output of multiple transistor stages to realize an amplifier with a bandwidth of more than a decade [1, 2]. While the bandwidth is wider than that of the single-stage wideband amplifier discussed in the previous section, the efficiency is much lower.

The topology of a four-stage distributed amplifier is shown in Figure 3-1(a). The distributed amplifier has two transmission lines, referred to as the gate line and drain line. Each stage includes an active device and two sections of transmission line, one being part of the gate line and the other being part of the drain line. The small-signal model of the input is shown in Figure 3-1(b) and that of the output in Figure 3-1(c). In the small signal model, the input of the transistor is modeled as a series resistance, $R_{i,n}$, and capacitance, $C_{gs,n}$, and these load the gate line. Ignoring $R_{i,n}$ for now, the small-signal input model is a transmission line that is loaded periodically by capacitors. This therefore appears as an artificial transmission line. If the line is terminated in an appropriate resistance, R_1, then no input signal is reflected at the end of the line segment. Proper design would result in very little power on the gate line after the final stage, as power is periodically coupled into the transistors. Design also ensures that there is a negligible backward-traveling wave on the input transmission line.

The small-signal model of the output drain line is similar, with a line periodically loaded by the output resistance and capacitance of the transistors. Now, however, there is a controlled current source that injects power onto the drain line. If there was only one stage, then the power delivered to the drain line would be split equally between forward- and backward-traveling components. However, here there are multiple stages, and the phase of the drain current injection changes along the line and current is preferably coupled into the forward-traveling wave. Still a termination resistor R_2 ensures that there is no backward-traveling wave on the drain line.

Power is periodically being tapped off of the gate line and an amplified signal is periodically inserted on the drain line. As a result, the transistors



(a) Distributed amplifier topology

(b) Small-signal input model (gate line)

(c) Small-signal output model (drain line)

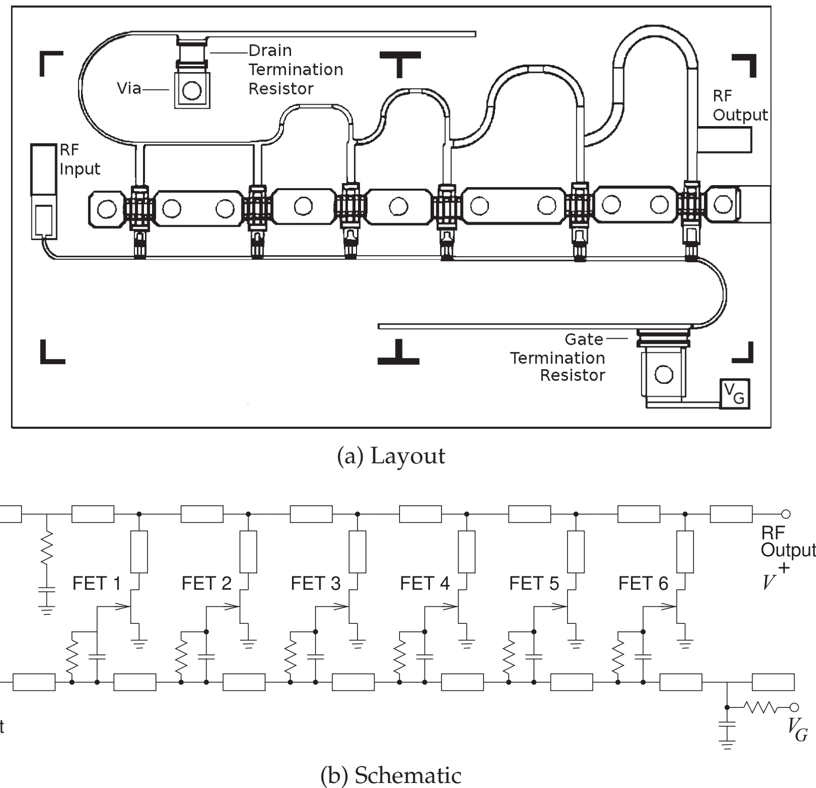
Figure 3-1: Distributed amplifier with four stages.

often are designed to increase in size along the length of the line. In this case the input and output capacitances of the transistors increase with each stage. Even if the transistors in each stage are of equal size, the characteristic impedances of the drain and gate transmission lines vary for each stage, and the lengths of the lines in the drain stage are not the same as the lengths of the lines in the gate line.

Distributed amplifiers can simplify stability constraints and enable amplification over multiple octaves. They also find application at millimeter-wave frequencies even when bandwidths of greater than one-half octave are not required [3]. At millimeter-wave frequencies parasitic capacitances are significant and these can be incorporated into the synthesis of the loaded transmission lines. Since the need to cancel parasitic capacitances is not required, it can be easier to achieve stable amplification.

3.3 Case Study: Analysis of a Distributed Amplifier

Figure 3-2(a) shows the layout of a monolithically integrated, large signal, distributed, GaAs power amplifier [4], model TGA8220 from Texas Instruments. The schematic of the amplifier is shown in Figure 3-2(b). This amplifier circuit is designed to deliver +25 dBm output power at 1 dB compression when operating from 2–18 GHz. Identical FETs are used in



(a) Layout

(b) Schematic

Figure 3-2: The TGA8220 MMIC distributed amplifier with six FETs (numbered 1–6 from the RF input). After [4], copyright *Microwaves & RF*, used with permission.

the six-stage amplifier and have a gate length $L = 0.5\ \mu\text{m}$ and gate width $W = 335\ \mu\text{m}$. Models of bends, tee junctions, vias, bond wires, and FET parasitics must be used. After bias and RF sources are defined, the circuit can be simulated in a nonlinear microwave simulator [5].

The small signal gain and the output power and efficiency at 1 dB gain compression are shown in Figure 3-3 with V_{DS} = 8 V and 50% I_{DSS}. The circuit was designed with series-gate capacitors to increase the gate-line cut-off frequency and to tailor the gate voltage excitation to maximize output power. Further gain and power enhancements were achieved with the help of tapered drain lines and a large drain termination resistor. This enables a 1 dB compressed output power of +25 dBm with a power added efficiency of 10% to be obtained over the 2–18 GHz band. The small-signal gain of at least 19 dB also has a small positive slope with frequency.

Nonlinear circuit simulation can also be used to understand the intuitive operation of the nonlinear circuit. This is particularly important for complex circuits such as this one, which uses FETs that are increasingly loaded by distributing them in a systematic manner. One particularly useful form of display that aids in understanding is the I-V phase plane, which is the locus of the I-V trajectory of an individual device's operating characteristic. The dynamic loadline of each FET in the amplifier at 18 GHz for 1 dB gain

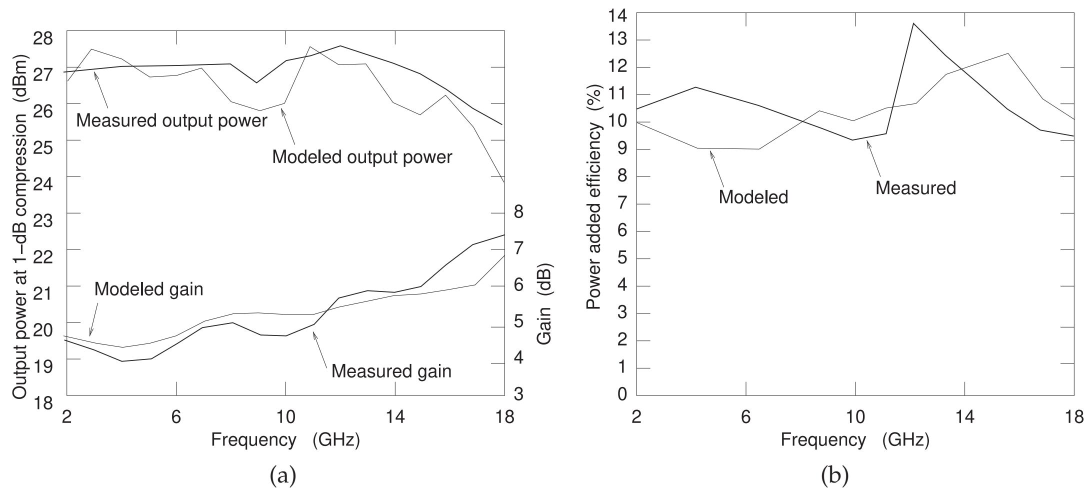


Figure 3-3: Gain, power, and efficiency of the TGA8220 MMIC distributed amplifier: (a) small-signal gain and output power at 1-dB compression; and (b) efficiency at 1-dB compression. After [4], copyright *Microwaves & RF*, used with permission.

compression at the output is given in Figure 3-4. The DC loadline (not shown) is a single line for each FET. The dynamic loadline opens up because of reactive loading. The match becomes better going from FET 1 to FET 6. Ideally the closed dynamic loadline would be achieved for all FETs, but there are many trade-offs required to achieve good gain, output power, and broad bandwidth. For efficiency, emphasis should be on maximizing the efficiency of the final stage, which operates at the highest power levels. The design here results in optimum output power across the entire bandwidth without unduly degrading the small-signal gain and input and output match for the remaining FETs in this amplifier. The use of series-gate capacitors and tapered drain lines is the mechanism that achieves this in this design [4]. A distributed amplifier delivers maximum output power and efficiency when each FET reaches gate and drain voltage limits for maximum power and efficiency simultaneously over a broad range of frequencies.

3.4 Negative Image Amplifier Design

Design using the negative image method is illustrated in the case study in Section 3.5 but here the philosophy behind the technique will be explained. The method breaks the stages the design in to much simpler steps.

In this section wideband amplifier design using the negative image method will be described for an amplifier having a single transistor. The idea can be applied to amplifier designs with multiple transistors. The basic model of a microwave transistor has shunt input and output capacitances and a feedback capacitance between the output and the input. A good amplifier design strategy would be to first place (ideal) negative capacitances in shunt with each of these capacitors and then attempt to synthesize a circuit that looks like a negative capacitor. This describes the essence of the negative image amplifier design method except that no attempt is made to directly

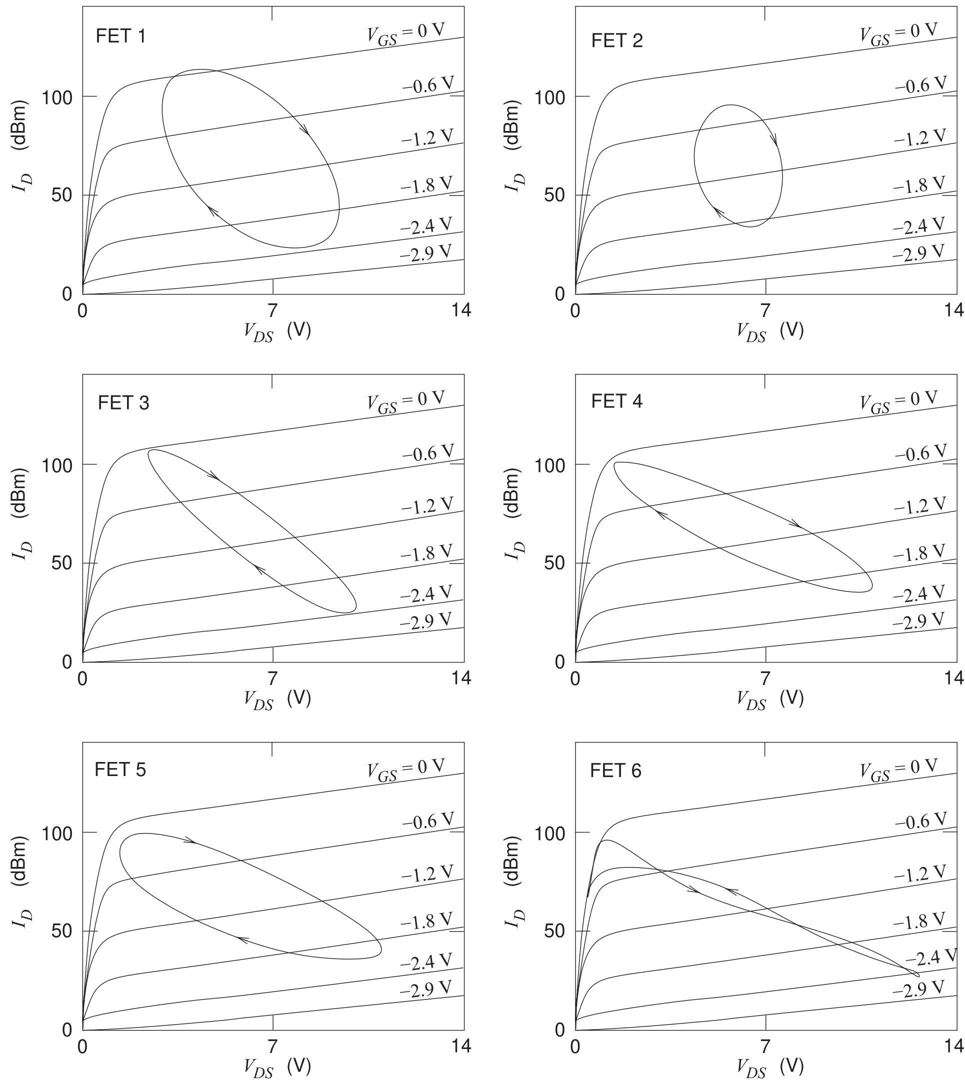


Figure 3-4: Dynamic loadlines of each FET in the TGA8220 MMIC distributed amplifier. After [4], copyright *Microwaves & RF*, used with permission.

cancel the transistor's feedback capacitor and instead the input and output matching networks are adjusted to account for it.

The negative image amplifier design method achieves high bandwidth by synthesizing input and output matching networks beginning with each network comprising a negative capacitance in parallel with the input and output, respectively, parasitic capacitances of the transistor. Then resistive loads, chosen for maximum power transfer, are put in parallel with the negative capacitances. This circuit is simulated with the actual model of the transistor and this is followed by an optimization step to optimize the broadband gain and noise responses of the amplifier while simultaneously ensuring stability of the amplifier. In this process the effect of the feedback

capacitance and the full complexity of the transistor are accounted for. The input and output matching networks are the negative image networks. The next step is to separately synthesize networks that provide the characteristics of the ideal input and output matching networks. This can only be done over a limited bandwidth but usually this is about half an octave. This process indicates the optimum characteristics of the input and output matching networks. The negative image networks can now be synthesized individually and once synthesized can be incorporated with the transistor model to obtain an overall circuit that can further be adjusted but perhaps only a few percent adjustment will be necessary.

The negative image method regularly achieves a half octave bandwidth. What is being done in the matching network design is using a topology that presents what looks like a negative capacitor and also the right impedance transformation (usually to 50 ohms). This is where invention comes into play. The impedance looking into the input (or output) of a transistor rotates with respect to frequency in the clockwise direction on a Smith chart. The complex conjugate impedance rotates in the counter-clockwise direction. The designer tries to develop a matching network that tracks the counter-rotating locus but with one capacitor and one inductor the impedance locus (with respect to frequency) looking into the matching network will rotate in the clockwise direction. The only simple circuit that will give you the right characteristics includes two or more transmission lines. The designer is using a topology that someone else discovered. It is not possible to synthesize the best network.

There are some limitations, both the input and output of the transistor will have some series inductance due to bondwires for discrete transistor parts and due to lengths of transmission line for on-chip transistors . The impedance of these inductances will be small compared to the parasitic capacitances and will really only matter if the input resistance of the transistor (in the case of the inductance at the input port) or the output resistance of the transistor (in the case of the inductance at the output port) is also small. Generally it is only necessary to compensate for the output inductance in the negative image model of the output network. and this is done by using use a negative inductance.

At this stage the amplifier design consists of input and output negative image matching networks which are quite simple and contain negative elements. The operation of the amplifier is optimized using these simple matching networks. The transistor is not unilateral so the input and output matching networks must be adjusted iteratively to get the optimum performance. The matching networks are so simple that manual tuning can be used in the circuit simulator..

With the simple matching networks designed, the challenge is now to realize the simple matching networks with real elements. L's and C's in a filter-like structure could possibly be used, but the result is rarely very good. The best results are obtained when transmission line structures are used. There is not a way to systematically synthesize these matching networks. The transmission line-based topologies that are used in the case study are inventions. There are very few other structures that work. The design problem is greatly simplified and design can focus on designing first the input matching network and then the output matching network without the transistor included.

3.5 Case Study: Wideband Amplifier Design

In this section an X-band wideband low-noise amplifier is designed.[1] The topology of the amplifier is shown in Figure 3-5, and this is the same topology used in narrowband amplifier design. The design specification is for a maximum noise figure (NF) of 1 dB and a gain of 14 ± 1 dB from 8 GHz to 12 GHz.

3.5.1 Transistor Properties

The transistor chosen is the packaged NEC NE32400A transistor and its parameters are given in Table 3-1 in what is called the Touchstone® format used by microwave simulators. The file begins with a number of comment lines (identified by '!') followed by the option line:

```
# <frequency unit> <parameter> <format> R <n>
```

where the `<frequency unit>` is GHz, <parameter> specifies the kind of network parameter data, and here S is scattering parameters. The <format>, MA, indicates that the data is in magnitude-angle(degrees) format, and the <n> term is 50, indicating that the S parameters are normalized to 50 Ω. The line of data is ordered as f, $|S_{11}|$, $\angle S_{11}$, $|S_{21}|$, $\angle S_{21}$, $|S_{12}|$, $\angle S_{12}$, $|S_{22}|$, and $\angle S_{22}$. The second set of data contains the noise parameters and there are five entries for each frequency arranged as frequency (using the previously specified units), the minimum noise figure $\mathrm{NF}_{\mathrm{min}}$ (in dB), then $|\Gamma_{\mathrm{opt}}|$, $\angle\Gamma_{\mathrm{opt}}$, and $r_n/50$. These are the noise parameters used with two-port amplifiers as described in Section 4.3.6 of [6] with $\mathrm{NF}_{\mathrm{min}} = 10\log(F_{\mathrm{min}})$ and Γ_{opt} being the reflection coefficient of Γ_{opt} referenced to Y_0 (= 0.02 S here).

The S parameters of the transistor are plotted in Figure 3-6. S_{11}, S_{12}, and S_{22} are plotted on a Smith chart in Figure 3-6(a). However, S_{21} is greater than one and so this is plotted on a polar plot in Figure 3-6(b). All of the S parameters vary significantly with frequency. In Figure 3-6(a) the locus of S_{11} from 8 GHz to 12 GHz is highlighted and the segment is labeled A. Ideal matching would require that the reflection coefficient, Γ_S, looking into the lossless input matching network from the transistor be the complex conjugate of S_{11} (if Port 2 of the transistor is terminated in 50 Ω).

[1] AWR Design Environment Project File: X_Band_LNA.emp

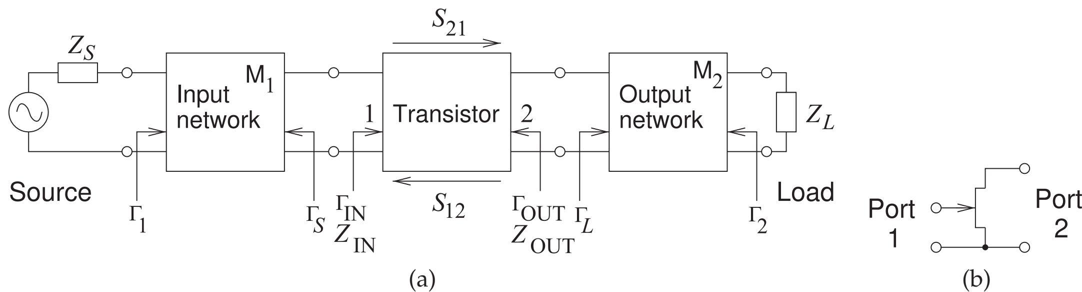
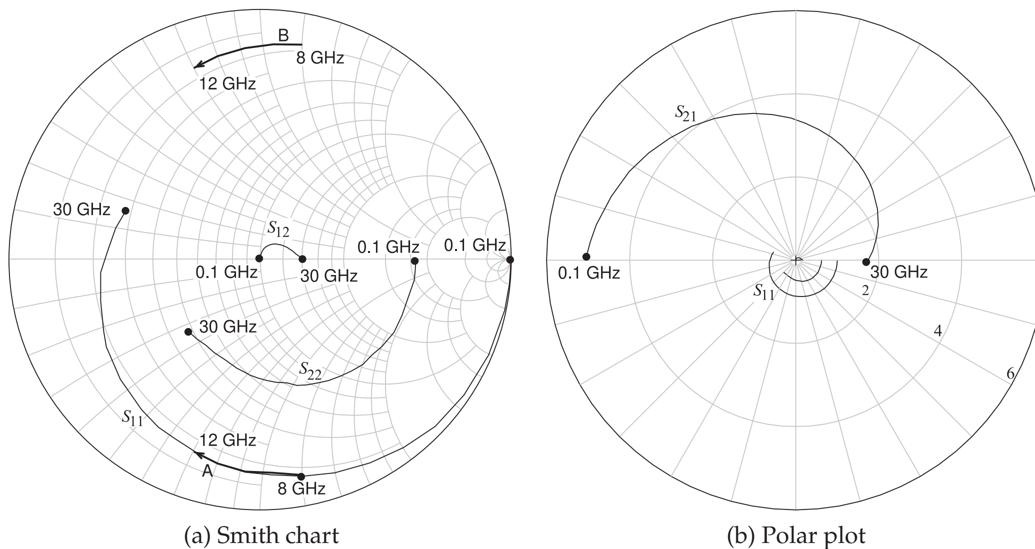


Figure 3-5: Wideband amplifier: (a) topology; and (b) port definition for transistor parameters.

Table 3-1: S parameter data file for a packaged NE32400A HJFET (heterojunction FET) transistor. `# GHZ S MA R 50` indicates frequency in GHz, S parameters in magnitude-angle(degrees) format, and reference to 50 Ω. The S parameter data are f(GHz), magnitude and angle of S_{11}, $|S_{21}|$, S_{12}, $|S_{22}|$. Noise data are f(GHz), $\mathrm{NF}_{\min}$ (dB), $|\Gamma_{\mathrm{opt}}|$, ang(Γ_{opt}) (in degrees), and $r_n/50$.

```
! FILENAME: N32400A.S2P VERSION: 5.0.
! NEC PART NUMBERS: NE32400 DATE:06/91
! BIAS CONDITIONS: VDS=2V, IDS=10mA
! NOTE: S-PARAMETERS INCLUDES BOND WIRES.
! GATE: TOTAL 2 WIRES, 1 PER BOND PAD, EACH WIRE 0.0132"(335um) LONG.
! DRAIN: TOTAL 2 WIRES, 1 PER BOND PAD, EACH WIRE 0.0094"(240um) LONG.
! SOURCE: TOTAL 4 WIRES, 2 PER SIDE, EACH WIRE 0.0070"(178um) LONG.
! WIRE: 0.0007"(17.8um) DIAMETER, GOLD
# GHZ S MA R 50
 0.1  .999    -1  5.04  179  .002  89  .62    -1
 0.2  .999    -3  5.02  178  .004  89  .62    -1
 0.5  .999    -6  4.97  175  .008  87  .62    -4
 1.0  .997   -12  4.88  170  .016  84  .62    -8
 2.0  .990   -23  4.70  161  .030  77  .61   -15
 3.0  .980   -34  4.54  152  .042  71  .61   -22
 4.0  .970   -44  4.38  144  .052  65  .61   -29
 5.0  .950   -53  4.22  136  .062  59  .60   -36
 6.0  .930   -62  4.08  128  .071  53  .59   -41
 7.0  .910   -71  3.93  120  .079  48  .59   -46
 8.0  .890   -79  3.80  113  .086  43  .58   -51
 9.0  .870   -87  3.67  106  .092  38  .57   -56
10.0  .860   -94  3.54   99  .099  34  .56   -61
11.0  .840  -102  3.42   92  .104  30  .55   -65
12.0  .820  -108  3.30   86  .109  27  .54   -70
13.0  .800  -115  3.19   80  .114  24  .53   -74
14.0  .790  -121  3.08   74  .119  21  .51   -78
15.0  .770  -128  2.97   68  .123  18  .50   -83
16.0  .750  -134  2.87   63  .127  16  .49   -87
17.0  .740  -139  2.77   57  .131  14  .48   -91
18.0  .720  -145  2.68   52  .135  12  .47   -95
19.0  .710  -150  2.59   47  .138  10  .46   -98
20.0  .690  -155  2.50   42  .142   8  .45  -102
22.0  .660  -165  2.32   32  .148   6  .43  -109
24.0  .640  -175  2.16   23  .153   4  .42  -116
26.0  .610   177  2.01   15  .159   3  .41  -122
28.0  .590   168  1.87    7  .163   1  .41  -128
30.0  .570   160  1.73   -1  .168   0  .41  -134
! NOISE PARAMETERS
! NOTE: NOISE PARAMETERS FOR 28 & 30 GHZ
! ARE EXTRAPOLATED, NOT MEASURED.
 1  0.30  .81    10  .39
 2  0.31  .79    17  .36
 4  0.33  .75    31  .33
 6  0.38  .72    45  .30
 8  0.43  .70    59  .27
10  0.50  .68    77  .24
12  0.60  .66    92  .22
14  0.71  .64   108  .19
16  0.85  .62   126  .18
18  1.00  .58   140  .15
20  1.20  .55   153  .13
22  1.50  .52   164  .11
24  1.80  .49   175  .10
26  2.10  .48  -176  .08
28  2.40  .46  -168  .07
30  2.80  .46  -160  .05
```



(a) Smith chart (b) Polar plot

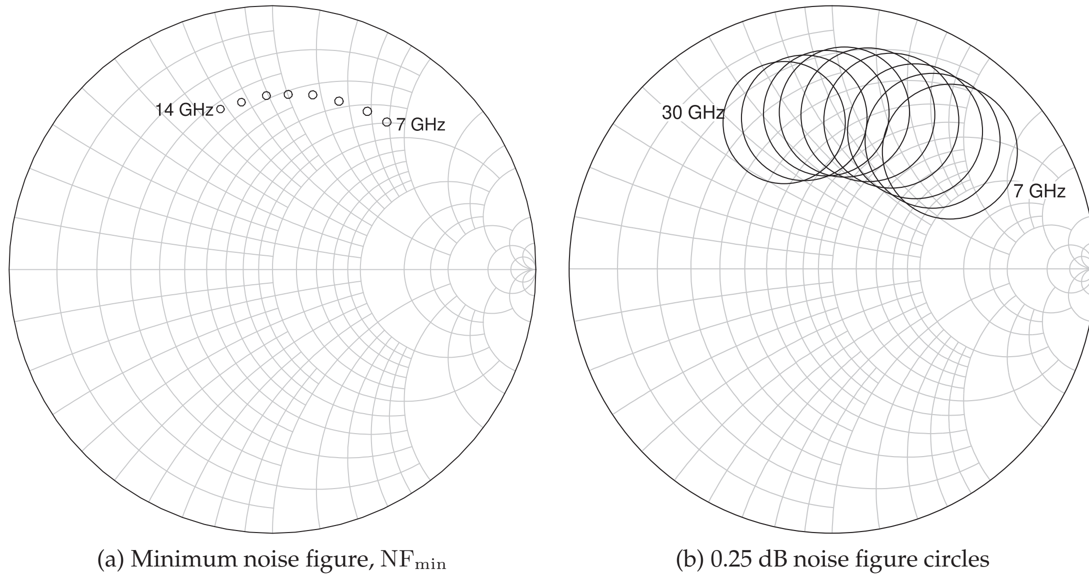
Figure 3-6: S parameters of the N32400A transistor. $|S_{21}|$ exceeds unity and is shown on a polar plot in (b) where 2, 4, and 6 indicate the magnitudes (radii) of constant $|\Gamma|$ circles.

Thus the locus of the optimum Γ_S is shown as segment B in Figure 3-6(a). Note that Γ_S rotates in the counterclockwise direction with increasing frequency. However, the input reflection coefficient of a simple matching network would rotate in the clockwise direction. Thus a reasonable match will only be achieved over a very narrow bandwidth. The output matching network situation is similar. The ideal matching network must have an input reflection coefficient that is counter to that of a simple network. So this illustrates the big difference between wideband and narrowband amplifier design. The matching networks must be designed to present the required complex conjugate impedance over a broad range of frequencies.

Another design task is simultaneously minimizing noise. The noise data of the transistor is plotted in Figure 3-7. Figure 3-7(a) plots the value of Γ_S $(= \Gamma_{\text{opt}})$ required to achieve the minimum noise figure. The points are just Γ_{opt} at different frequencies. These points do not coincide with the Γ_S for optimum matching as shown in Figure 3-6(a). So a compromise is needed. This compromise step is guided by the noise figure circles. Figure 3-6(b) plots the noise figure circles when the noise figure is 0.25 dB higher than NF_{min}. For example, at one frequency, if Γ_S is on the circle for that frequency, the noise figure will be 0.25 dB higher than NF_{min}. If Γ_S is inside the circle the noise figure will be less than 0.25 dB above NF_{min}.

A more complete set of noise figure circles at 10 GHz, the middle of the amplifier band, is shown in Figure 3-8. NF_{min} is 0.50 dB and the noise figure circles are in 0.1 dB steps.

Another consideration affecting the choice of matching networks is the stability of the amplifier. The input and output stability circles for the transistor are shown in Figure 3-9 starting at 2 GHz and up to 30 GHz. For the transistor to be unconditionally stable, Γ_S, must lie in the unconditionally stable region of the Smith chart. The stable regions are shown in Figure



(a) Minimum noise figure, $\mathrm{NF_{min}}$

(b) 0.25 dB noise figure circles

Figure 3-7: Noise characteristic from 7 to 14 GHz in 1 GHz steps plot on the input (Γ_S) plane. $\mathrm{NF_{min}}$ = 0.38 dB, 0.41 dB, 0.43 dB, 0.47 dB, 0.50 dB, 0.55 dB, 0.60 dB, 0.66 dB, and 0.71 dB from 7 to 14 GHz in 1 GHz steps. The noise figure on each circle is $\mathrm{NF_{min}} + 0.25$ dB.

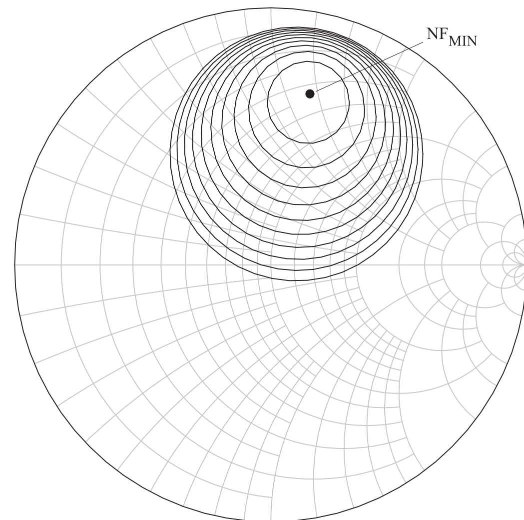
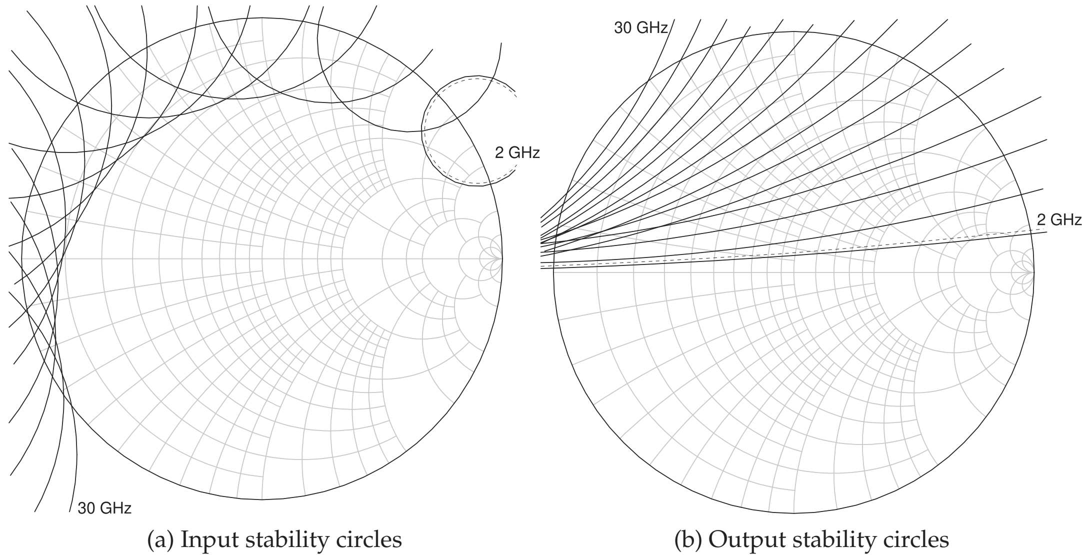


Figure 3-8: Noise figure circles at 10 GHz where $\mathrm{NF_{min}} = 0.50$ dB. Circles have 0.1 dB steps so that the inner-most circle indicates the values of Γ_S that achieve NF = 0.6 dB.

3-9(a) at all frequencies. Similarly, Γ_L must lie in the stable region of the Smith chart in Figure 3-9(b) at all frequencies. The final consideration is the maximum available gain, G_{MAX}. The G_{MAX} circles are shown in Figure 3-10. At 8 GHz $G_{\mathrm{MAX}} = 16.6$ dB and it reduces to 14.8 dB at 12 GHz. This further complicates design as the gain of the final amplifier should be flat across the band and not monotonically decreasing.

So the complete design problem is to determine the matching network topology and then develop the input and output matching networks that meet all of the constraints implied by the stability circles, the noise figure



(a) Input stability circles (b) Output stability circles

Figure 3-9: Stability circles in 2 GHz steps starting at 2 GHz and continuing up to 30 GHz. The potentially unstable region is indicated by the dashed line on the 2 GHz circle.

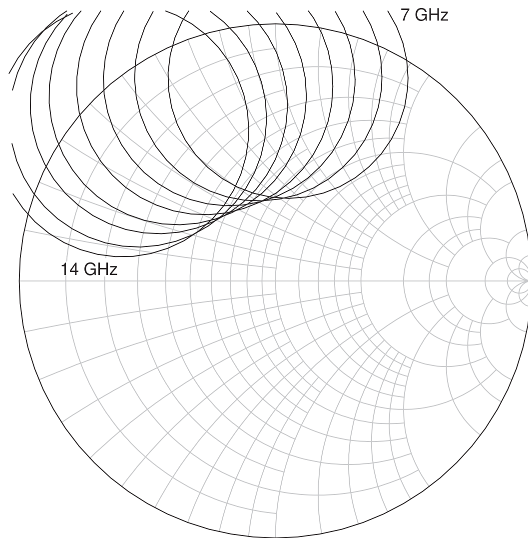


Figure 3-10: Maximum available gain, G_{MAX}, circles. $G_{\mathrm{MAX}} = 17.0$ dB, 16.5 dB, 16.0 dB, 15.5 dB, 15.2 dB, 14.8 dB, 14.5 dB, 14.1 dB at 7 to 14 GHz in 1 GHz steps.

circles, and the G_{MAX} circles.

3.5.2 Negative Image Design

A successful strategy for wideband design is the negative image amplifier design technique. The development begins by considering the fundamental input and output impedances of the transistor. The input of a transistor can be approximated as a resistance in series with a capacitance. The output of the transistor appears as a capacitance in parallel with a resistance. So a simple matching strategy is to consider an input matching network that presents a negative series capacitance (the image) to the

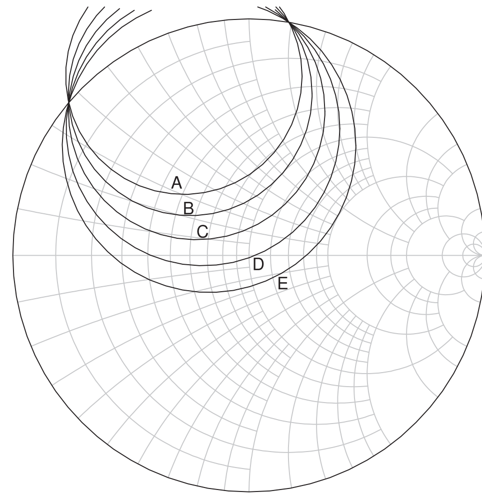
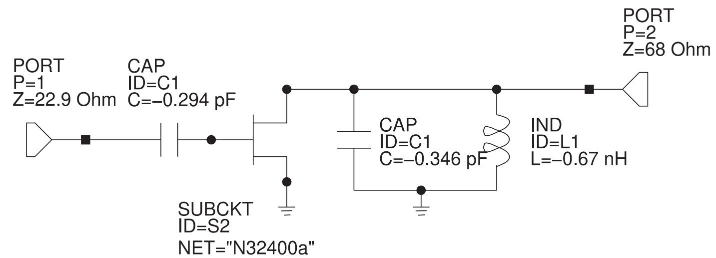
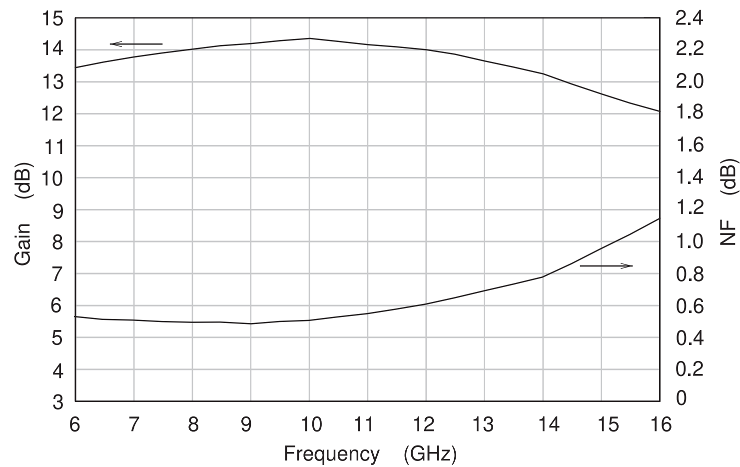


Figure 3-11: Maximum available gain, G_{MAX}, circles at 10 GHz in 1 dB steps. The central circle has G_{MAX} =15.5 dB.



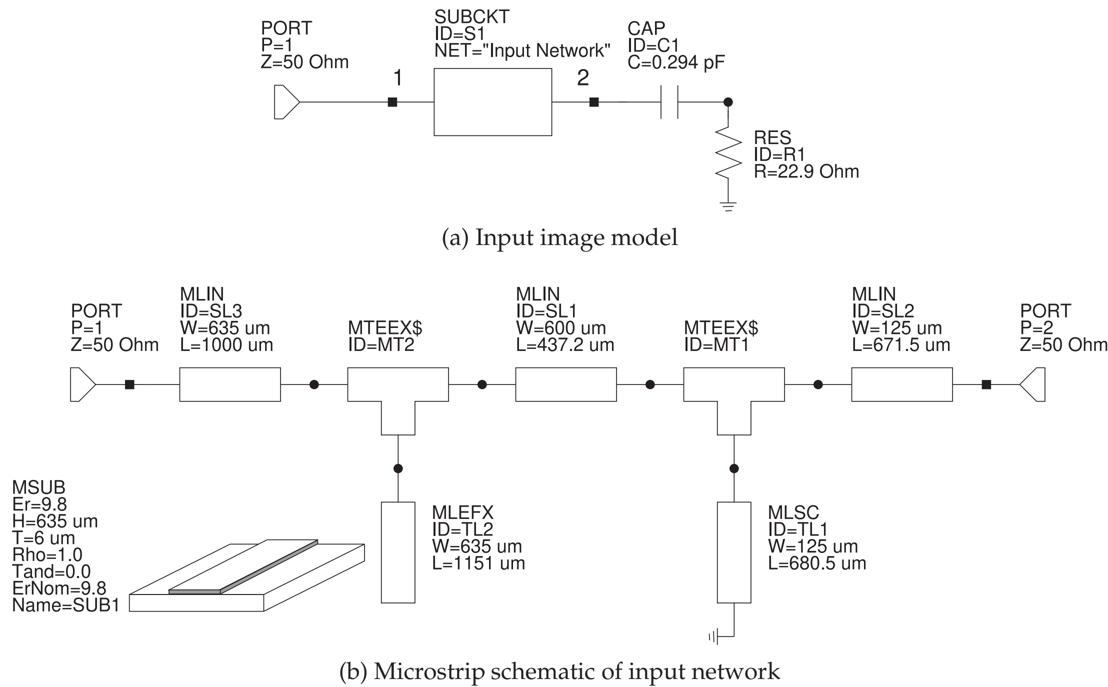
(a) Image amplifier schematic.



(b) Gain and noise figure of the image amplifier.

Figure 3-12: Amplifier using negative image model.

input of the transistor and a negative shunt capacitance to the output of the transistor. Such an amplifier is shown in Figure 3-12(a). The output matching network also includes a negative shunt inductance that cancels the bondwire inductance of the packaged transistor. The input and output port impedances were adjusted to achieve the required gain. The values of the input and output port impedances as well as of the three reactive elements can be optimized or adjusted using the manual tuning feature in most microwave simulators. Tuning is a useful feature that provides considerable



(a) Input image model

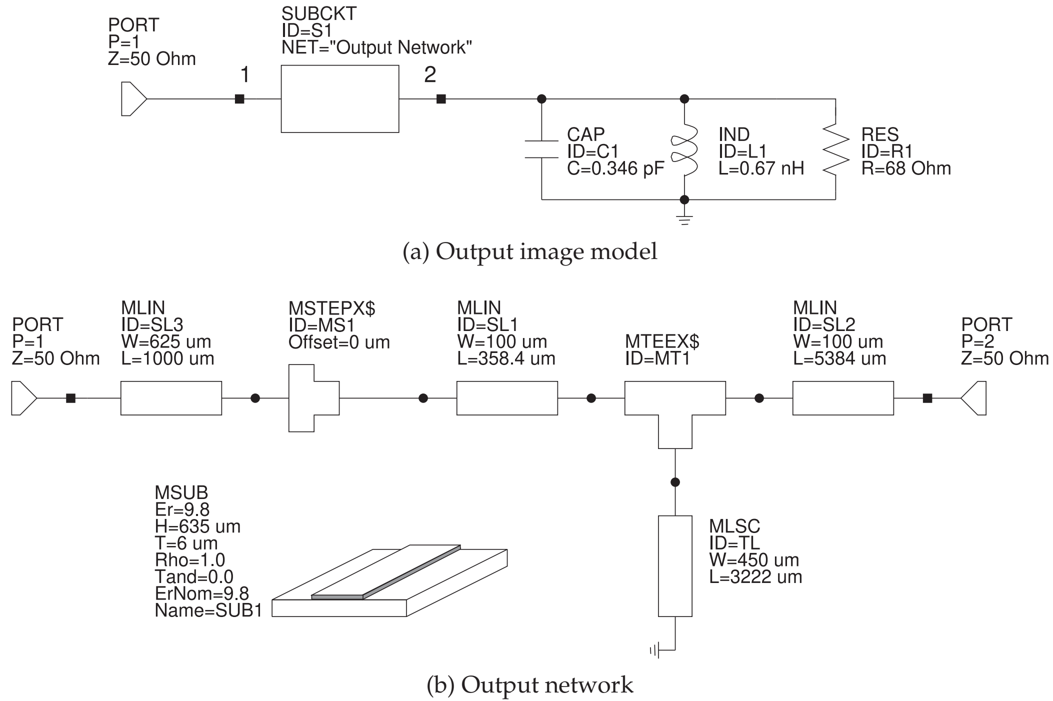
(b) Microstrip schematic of input network

Figure 3-13: Microstrip realization of the input matching network using a microstrip substrate, MSUB. The layout begins with a port element PORT 1 (P=1) with a reference impedance of 50 Ω. The MLIN element is a microstrip line with width W and length L; the MTEEX$ element models a microstrip tee and supports the shunt connection of the MLEFX element, which is an open-circuited microstrip line with end effects modeled; another line and tee connects a shorted stub, the MLSC element; then another line; and finally a second PORT element.

insight. The trade-offs are not always easy to make without using the image amplifier technique.

The noise and gain of the image amplifier of Figure 3-12(a) are shown in Figure 3-12(b). While the gain and noise figure do not meet the specification (13 dB gain and NF < 1 dB), they are very close and it can be expected that optimization will achieve the required design.

At this stage the topologies of the input and output matching networks need to be selected since negative inductances and capacitors are not available. There are several ways this can be done. One way is to develop transfer function descriptions of the impedances of the input (and output) network seen from the transistor. The impedance functions can then be synthesized and developed as if they were filters. This can be a long process, but sometimes it is the only way to meet demanding specifications. Very often the topology can be adopted from an earlier design or from a design reported in a publication. The topology chosen here for the input network is shown in Figure 3-13(b). (The theory behind this topology is described in Section 7.7 of [6].) The parameters of the input matching network are optimized using the input image model shown in Figure 3-13(a). However, the sign of the negative capacitance in the input circuit of Figure 3-12(a) is changed. The series connection of the 0.294 pF capacitor in series with



(a) Output image model

(b) Output network

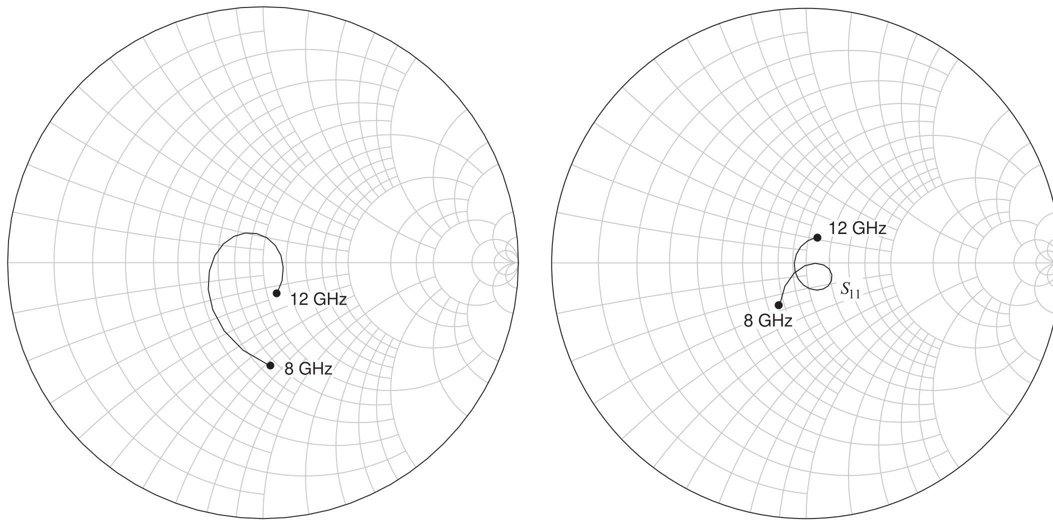
Figure 3-14: Realization of the output network.

the 22.9 Ω resistor approximates the input impedance of the (terminated) transistor. More specifically, it is the impedance that will result in the gain and noise profile in Figure 3-12(b). The goal in realizing the input matching network is to minimize the input reflection coefficient (normalized to 50 Ω) at the input port. A similar approach is used in developing the output matching network, shown in Figure 3-14. Following optimization, the input reflection coefficients at Port 1 of the matching networks terminated in the image networks are shown in Figure 3-15.

3.5.3 Final Design

The input and output matching networks are connected to the transistor as shown in Figure 3-16 and then the complete amplifier is optimized. The parameters of the optimized input and output matching networks using the complete transistor model are given in Figures 3-13(b) and 3-14(b), and the complete layout is shown in Figure 3-17. The gain and noise performance of the completed design is given in Figure 3-18. This wideband amplifier topology achieves a bandwidth up to one-half octave (e.g. 8–12 GHz).

In some cases, although not required here, it is necessary to introduce feedback from the output to the input of the transistor. This is often a simple circuit such as a cascade of a capacitor, an inductor, and a transmission line. The feedback network provides frequency-dependent feedback that flattens the gain response. A resistor can be also included in the feedback network to manage stability.



(a) Γ_{in} of the input network, in Figure 3-13 (b) Γ_{in} of the output network, in Figure 3-14

Figure 3-15: Reflection coefficient looking into Port 1 of the input and output matching networks terminated in the corrected image network.

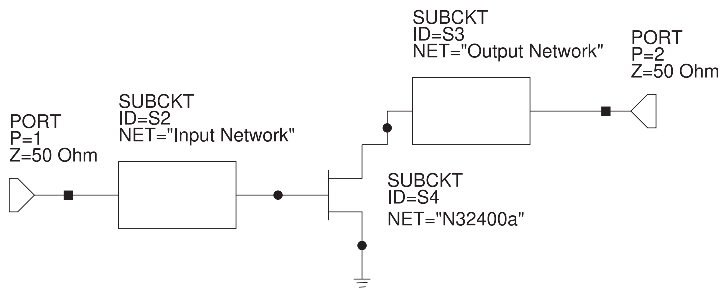


Figure 3-16: Final amplifier.

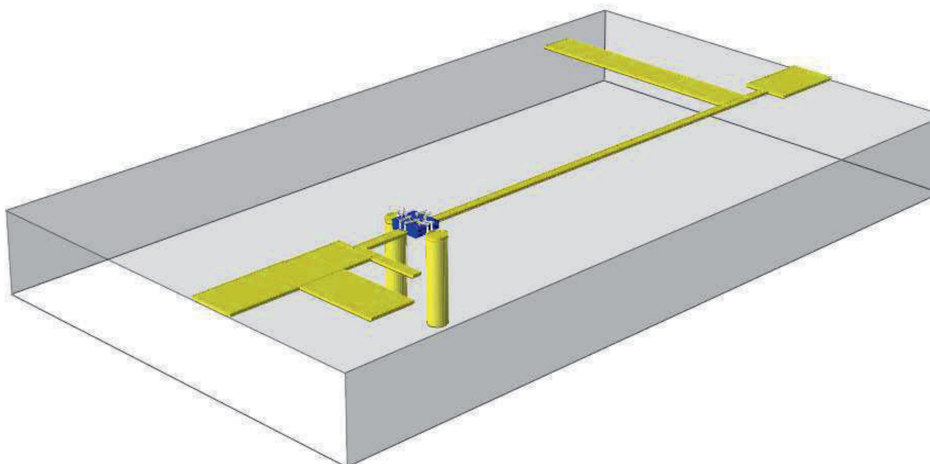


Figure 3-17: Final layout of the X-band LNA. The input is on the left and the output on the right.

3.6 Differential Amplifiers

A significant change in RF and microwave engineering has been the increasing importance of differential circuits such as the amplifier in Figure 3-19(a). In part this is because they are conveniently implemented in silicon technology. It is also a result of the use of monolithic integration and the maturity of semiconductor technologies resulting in repeatable RF active components. Differential amplifiers are the preferred amplifier topology with RFICs. Since substrate noise is common to all nodes of a differential amplifier, there is little differential substrate noise signal. Also, differential circuits lend themselves to current-mode biasing which is preferred on-chip. The defining characteristic of a differential amplifier is that there are paired signal paths that are differential. These amplifiers are also (but less commonly) called **balanced amplifiers**. When the RF signal on one side of the differential path is positive, the RF signal on the other side is negative.

3.6.1 Fully and Pseudo-Differential Amplifiers

Figure 3-19(a) shows a **fully differential amplifier** (**FDA**) with resistive biasing in the drain legs. As well as providing biasing current, the resistors load the amplifier. The supply voltage of an RFIC can be quite low (a few volts or less), so choosing circuit topologies that provide for large voltage swings is important, particularly for a driver amplifier being the last

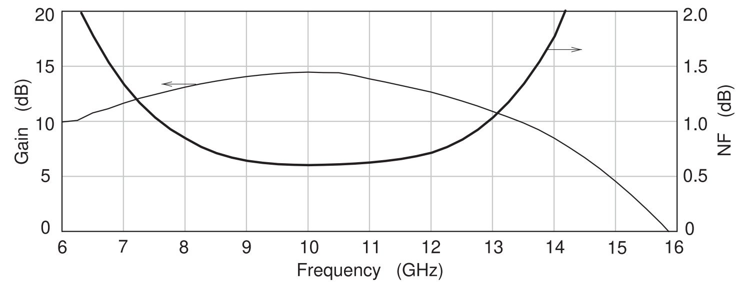


Figure 3-18: Final amplifier performance.

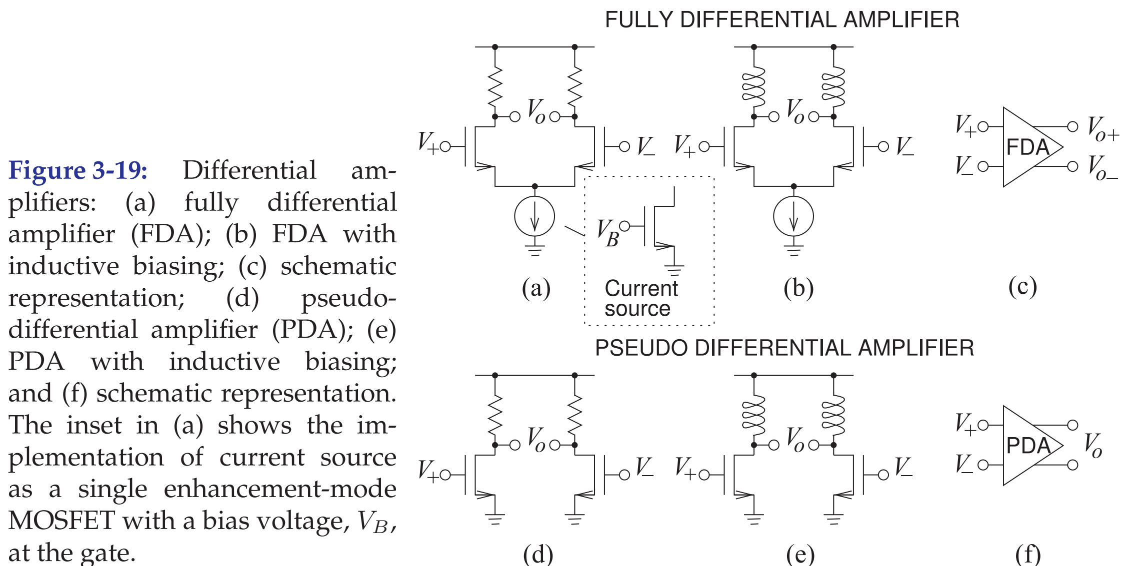


Figure 3-19: Differential amplifiers: (a) fully differential amplifier (FDA); (b) FDA with inductive biasing; (c) schematic representation; (d) pseudo-differential amplifier (PDA); (e) PDA with inductive biasing; and (f) schematic representation. The inset in (a) shows the implementation of current source as a single enhancement-mode MOSFET with a bias voltage, V_B, at the gate.

amplifier stage in a transmitter RFIC that drives a following power amplifier. Differential topologies lead to an almost doubling of the output voltage swing compared to the output voltage swing of a single-ended amplifier. An FDA includes a common current source that can be implemented quite simply using a single FET, as shown in the inset in Figure 3-19(a). Here the gate-source voltage is the bias voltage, V_B, which, from Figure 2-9(b), establishes a nearly constant drain current as long as there is sufficient drain-source voltage across the current source transistor.

Common-Mode Rejection

One of the attributes that makes FDAs attractive is that they are relatively immune to substrate noise (noise in the substrate produced by other circuits). The signal applied to the inputs of a differential amplifier have differential- and common-mode components. Referring to the differential amplifier in Figure 3-19(c), the differential-mode input signal is

$$V_{id} = V_+ - V_- \tag{3.1}$$

and the common-mode input signal is

$$V_{ic} = \tfrac{1}{2}(V_+ + V_-). \tag{3.2}$$

Similarly the differential- and common-mode output signals are

$$V_{od} = V_{o+} - V_{o-} \quad \text{and} \quad V_{oc} = \tfrac{1}{2}(V_{o+} + V_{o-}), \tag{3.3}$$

respectively. The differential-mode voltage gain is

$$A_d = \frac{V_{od}}{V_{id}} \tag{3.4}$$

and the common-mode gain is

$$A_c = \frac{V_{oc}}{V_{ic}}. \tag{3.5}$$

For good noise immunity, the common-mode gain should be low and the differential-mode gain should be high. The figure of merit that describes this is the **common-mode rejection ratio** (**CMRR**):

$$\text{CMRR} = \frac{A_d}{A_c}, \tag{3.6}$$

and the larger this is, the better. CMRR is usually expressed in decibels, and since CMRR is a voltage gain ratio, CMRR in decibels is $20\log(A_d/A_c)$. The current source at the source of the differential pair of the FDA has a large effect on the CMRR by suppressing the output common-mode voltage. Then the current source results in a large CMRR. Without the current source, the CMRR of the FDA of Figure 3-19(a) would be one.

Output Voltage Swing

Single-ended amplifiers were discussed in Section 2.5.1, where it was shown that inductive biasing enables higher output voltage swings than possible

with resistive biasing. A similar enhancement can be obtained with a differential amplifier. The inductively biased FDA of Figure 3-19(b) has a higher voltage swing than the resistively biased FDA of Figure 3-19(a). More can be achieved, however. The current sources at the common source point of the FDAs in Figure 3-19(a and b) limit the voltage swing, as there is a minimum drain-source voltage drop required across the current source for it to maintain constant current. When larger output voltage swings are required, the current source is eliminated and the resulting amplifier is called a **pseudo-differential amplifier** (PDA), as shown in Figure 3-19(d). Again, inductive biasing (see Figure 3-19(e)) almost doubles the possible voltage swing. The performance cost with the PDA circuit is that the CMRR is one.

The output voltage waveforms for single-ended and differential amplifiers with and without inductive biasing are shown in Figure 3-20. The inductively biased PDA, shown in Figure 3-20(d), has an output voltage swing that is about 4 times the voltage swing (or about 16 times the power into the same load) of the single-ended resistively biased Class A amplifier in Figure 3-20(a) (the actual factors depend on the supply voltage and $V_{DS,\min}$).

EXAMPLE 3.1 Calculation of Common-Mode Rejection Ratio

Determine the CMRR of the FET differential amplifier shown in Figure 3-21(a).

Solution:

The strategy for solving this problem is to develop the common-mode and differential-mode equivalent circuits and solve for the gain of each. The first step is to develop the small-signal model shown in Figure 3-21(b). The differential input signal is V_{id} and the common input signal is V_{ic} so that the input voltage signals are

$$V_{i+} = \tfrac{1}{2}\left(V_{id} + V_{ic}\right) \quad \text{and} \quad V_{i-} = -\tfrac{1}{2}\left(V_{id} + V_{ic}\right). \tag{3.7}$$

The expressions are similar for the output differential- and common-mode signals V_{od} and V_{oc}. This leads to the small signal differential-mode model of Figure 3-21(c) and the small signal common-mode model of Figure 3-21(d). From Figure 3-21(c), the output differential signal is

$$V_{od} = \frac{V_{id}}{2}\left[-g_m(r_d//R_L)\right] - \frac{-V_{id}}{2}\left[-g_m(r_d//R_L)\right] = \frac{-V_{id}g_m r_d R_L}{r_d + R_L}, \tag{3.8}$$

so the differential gain is

$$A_d = \frac{V_{od}}{V_{id}} = \frac{-g_m r_d R_L}{r_d + R_L}. \tag{3.9}$$

If, as usual, $r_d \gg R_L$, this becomes

$$A_d = -g_m R_L. \tag{3.10}$$

Focusing on the small signal common-mode model of Figure 3-21(d) yields the output common-mode signal. The two halves of the circuit are now identical. The sum of the currents at X is zero, so

$$\frac{V_S}{2R_S} + \frac{V_S - V_{oc}}{r_d} - g_m(V_{ic} - V_S) = 0, \tag{3.11}$$

and the sum of the currents at the output terminal is zero, so

$$\frac{V_{oc}}{R_L} + \frac{V_{oc} - V_S}{r_d} + g_m(V_{ic} - V_S) = 0. \tag{3.12}$$

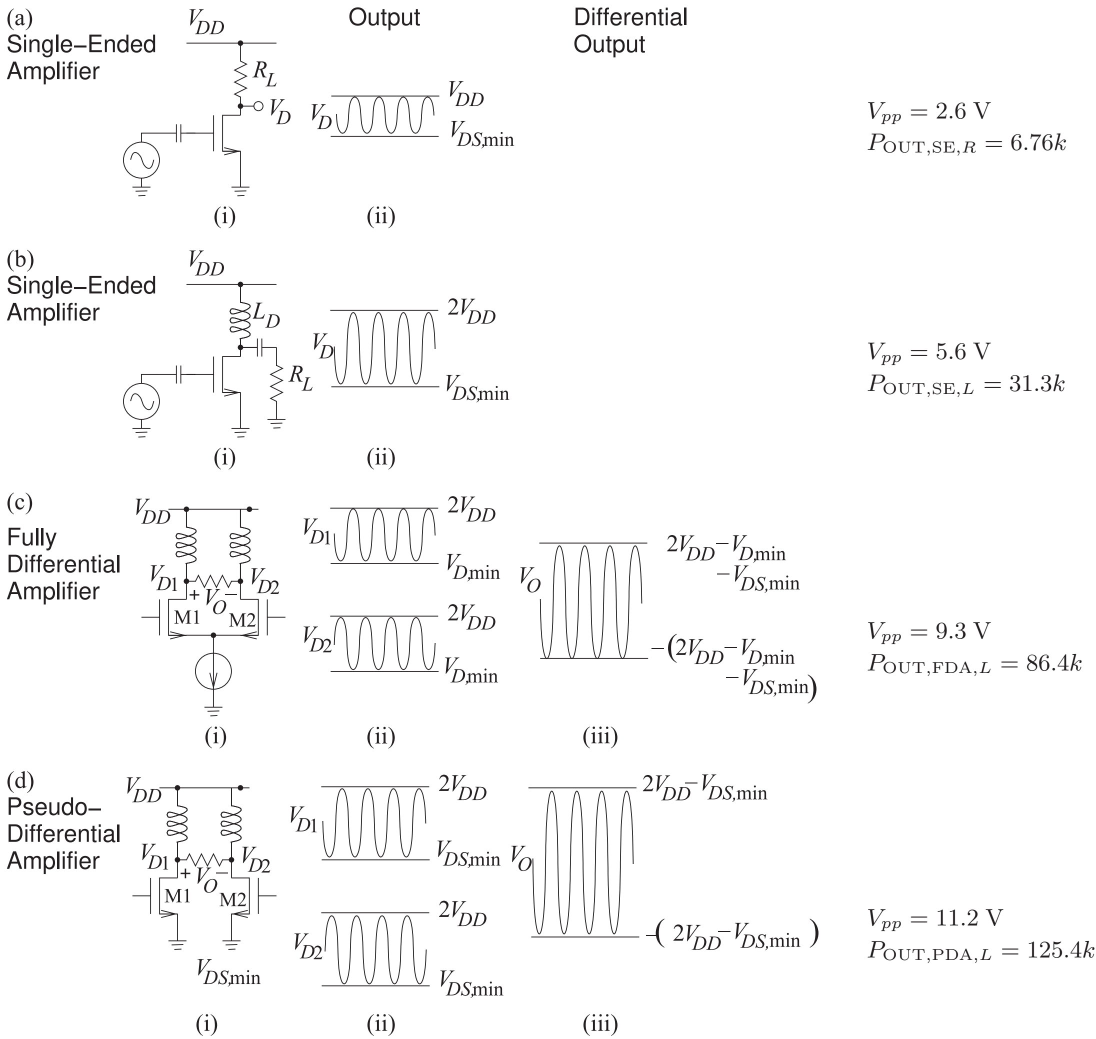


Figure 3-20: Class A MOSFET amplifiers with output voltage waveforms: (a) single-ended amplifier with resistive biasing; (b) single-ended amplifier with inductive biasing; (c) fully differential amplifier with inductive biasing; and (d) pseudo-differential amplifier. Schematic is shown in (i), drain voltage waveforms in (ii), and differential output in (iii). The final column gives the output voltage swing, V_{pp}, and the output power with $V_{DD} = 3$ V, $V_{D,\text{min}} = 0.95$ V, $V_{DS,\text{min}} = 0.4$ V, and k is a proportionality constant dependent on loading that is assumed to be the same for all amplifiers. $V_{D,\text{min}}$ is the minimum voltage at the drain of the current-source MOSFET. The resistively biased single-ended amplifier has an output power proportional to 6.76 while the inductively biased PDA in (d) has an output power proportional to 125.4, 18.6 times larger.

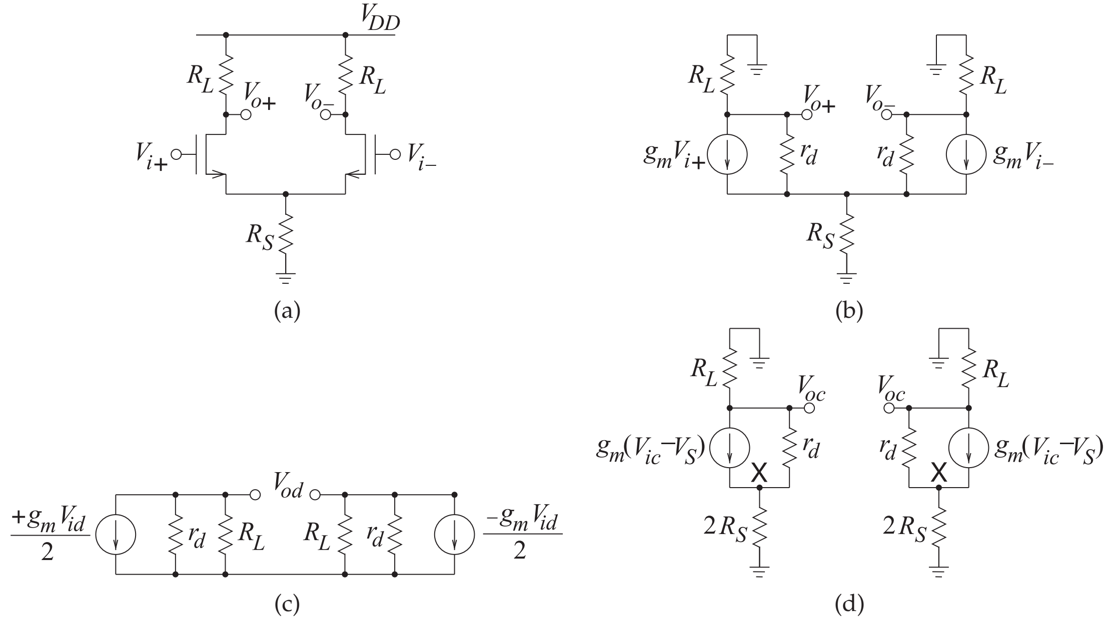


Figure 3-21: Differential amplifier: (a) schematic; (b) small signal model; (c) small signal model for calculating differential gain; and (d) small signal model for calculating common-mode gain.

Eliminating V_S from these equations leads to

$$V_{oc} = \frac{-g_m r_d R_L V_{ic}}{(1 + g_m r_d)2R_S + r_d + R_L}, \quad (3.13)$$

so the common-mode gain is

$$A_c = \frac{V_{oc}}{V_{ic}} = \frac{-g_m r_d R_L}{(1 + g_m r_d)2R_S + r_d + R_L}. \quad (3.14)$$

If, as usual, $r_d \gg R_L$, this becomes

$$A_c = \frac{-g_m R_L}{1 + 2g_m R_S}. \quad (3.15)$$

The CMRR (when $r_d \gg R_L$) is

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{-g_m R_L(1 + 2g_m R_S)}{-g_m R_L} = (1 + 2g_m R_S). \quad (3.16)$$

So the CMRR depends on the value of R_S. If there is no resistor at the common-mode source point, as in a pseudo-differential amplifier, $R_S = 0$ and so

$$\text{CMRR}|_{R_S=0} = 1. \quad (3.17)$$

If there is an ideal current source at the source node, then R_S is effectively infinite, and so

$$\text{CMRR}|_{\text{current source}} = \infty. \quad (3.18)$$

3.6.2 Even, Common, Odd, and Differential Modes

The difference between even- and common-mode current, voltages and impedances comes down to bookkeeping as to how the voltages and currents are defined. The same is true for the odd- and differential-mode quantities. The reason both sets of definitions are used is because the even-/odd-mode set usage is preferred with transmission line structures and the common-/differential-mode set usage is preferred with complementary transistor circuits such as differential amplifiers.

Consider the amplifier shown in Figure 3-22(a) with two inputs and two outputs. The input and output voltages in the various modes are defined as follows:

Odd-mode input voltage, V_{io}, and current, I_{io} (with the second subscript indicating the mode):

$$V_{io} = \tfrac{1}{2}\left(V_{i1} - V_{i2}\right), \quad \text{and} \quad I_{io} = \tfrac{1}{2}\left(I_{i1} - I_{i2}\right). \tag{3.19}$$

Differential-mode input voltage, V_{id}, and current, I_{id}:

$$V_{id} = \left(V_{i1} - V_{i2}\right), \quad \text{and} \quad I_{id} = \tfrac{1}{2}\left(I_{i1} - I_{i2}\right). \tag{3.20}$$

Even-mode input voltage, V_{ie}, and current, I_{ie}:

$$V_{ie} = \tfrac{1}{2}\left(V_{i1} + V_{i2}\right), \quad \text{and} \quad I_{ie} = \tfrac{1}{2}\left(I_{i1} + I_{i2}\right). \tag{3.21}$$

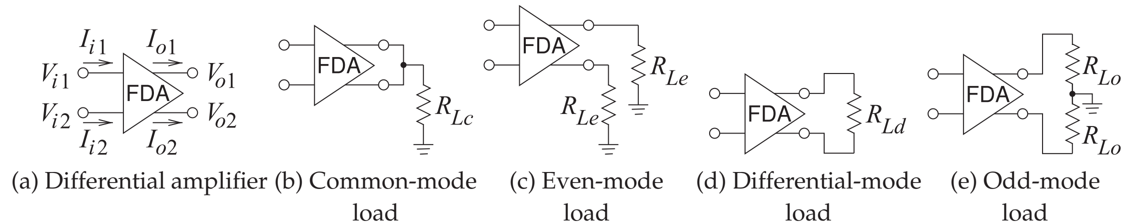
Common-mode input voltage, V_{ic}, and current, I_{ic}:

$$V_{ic} = \tfrac{1}{2}\left(V_{i1} + V_{i2}\right), \quad \text{and} \quad I_{ic} = \left(I_{i1} + I_{i2}\right). \tag{3.22}$$

Reversing the definitions, if there is no common-/even-mode input signal:

$$\begin{array}{lll} V_{i1} = \tfrac{1}{2}V_{id} = V_{io}, & & V_{i2} = -\tfrac{1}{2}V_{id} = -V_{io}, \\ I_{i1} = I_{id} = I_{io}, & \text{and} & I_{i2} = -I_{id} = -I_{io}. \end{array} \tag{3.23}$$

The output voltages and currents are similarly related. Figures 3-22(b)–3-22(e) show the conceptual even-, odd-, common- and differential- mode load definitions. In switching between definitions, say between the differential load and the odd-mode load, the actual resistor in the circuit does not change.

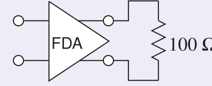


(a) Differential amplifier (b) Common-mode load (c) Even-mode load (d) Differential-mode load (e) Odd-mode load

Figure 3-22: Differential amplifiers and various loads. R_{Lc} is the common-mode load, R_{Le} is the even-mode load, R_{Ld} is the differential-mode load (often the term differential load is used), and R_{Lo} is the odd-mode load.

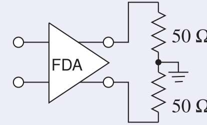
EXAMPLE 3.2 Odd-Mode Load

The differential amplifier to the right has a differential load of 100 Ω. What is the odd-mode load?



Solution:

The circuit is put into the odd-mode form to the right. Comparing this to the load definitions shown in Figure 3-21(d), it is seen that the odd-mode load impedance is 50 Ω.



3.6.3 Asymmetrical Loading

It is simple enough to determine the common and differential loads, or similarly the even- and odd-mode loads, when the loading of a differential amplifier is symmetrical. However when loading is asymmetrical, details of the driving differential amplifier are required to determine the coupling between the common and differential signals. The situation is similar to that with a terminated coupled line, see Section 5.7 of [7], where the Thevenin equivalent impedance of the source is required to determine the circuit conditions.

With an asymmetrical load there will be coupling between the even and odd modes. So even if the driving differential amplifier produces a differential output current and has zero common mode current, there could still be a common mode voltage. This is important as transistors operate as voltage-controlled current sources and many differential amplifiers are actually transconductance amplifiers as this gives the widest bandwidths, simplest biasing, and good noise immunity. The output stage of a differential amplifier appears as differential voltage-controlled current sources and in an RFIC adaptive mechanisms usually ensure that there is no common-mode current. But the differential current can induce a common-mode voltage which drives following stages. The design strategy then is to ensure that a differential amplifier produces minimal common-mode current, and loading is symmetrical. The following examples are illustrative.

EXAMPLE 3.3 Asymmetrical Loading of a Differential Amplifier

A differential amplifier has two output terminals with one of the outputs connected to a 60 Ω resistor and the other terminated in a 100 Ω resistor, as shown in Figure 3-23(a). The output stage of the differential amplifier is modeled as two controlled current sources I_{o1} and I_{o2} and the output common-mode current is zero.

(a) What is the common-mode voltage, V_c, at the load if the differential current is 1 mA?
This problem will first be solved using the general loads shown in Figure 3-23(b). The voltages at the load are $V_{o1} = V_c + \frac{1}{2}V_d$ and $V_{o2} = V_c - \frac{1}{2}V_d$ where V_d is the differential output voltage. The output currents are $I_{o1} = \frac{1}{2}I_c + I_d = I_d$ and $I_{o2} = \frac{1}{2}I_c - I_d = -I_d$. Then

$$V_{o1} = V_c + \tfrac{1}{2}V_d = I_{o1}R_1 = +I_dR_1 \tag{3.24}$$

$$V_{o2} = V_c - \tfrac{1}{2}V_d = I_{o2}R_2 = -I_dR_2 \tag{3.25}$$

combining these

$$2V_c = I_d(R_1 - R_2), \quad \text{and so} \quad V_c = \tfrac{1}{2}(1\ \text{mA}(60\ \Omega - 100\ \Omega) = 40\ \text{mV}. \tag{3.26}$$

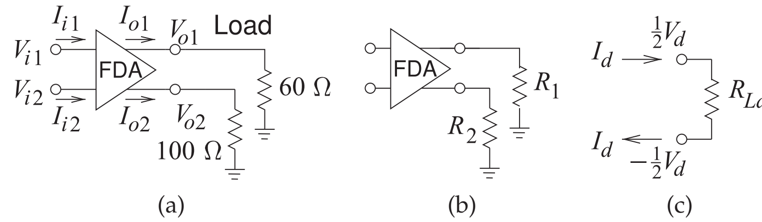


Figure 3-23: Terminated differential amplifier: (a) asymmetrical loading; (b) general representation of loading; and (c) definition of voltages and currents for the differential-mode load impedance R_{Ld}.

The common mode voltage at the output is 40 mV.

(b) What is the differential-mode load resistance, R_{Ld}?
The differential-mode load R_{Ld} is defined in Figure 3-23(d) so that $R_{Ld} = V_d/I_d$. Taking the difference of Equations (3.24) and (3.25) and eliminating V_c leads to

$$V_d = I_d(R_1 + R_2) + \tfrac{1}{2}I_c(R_1 - R_2) \quad \text{and} \quad R_{Ld} = \frac{V_d}{I_d} = (R_1 + R_2) = 160\ \Omega. \tag{3.27}$$

EXAMPLE 3.4 Differential- and Odd-Mode Loads

A differential amplifier is shown in Figure 3-24(a) with resistive loading. Find the differential- and odd-mode load resistances if the common-mode current is zero.

Solution:

Nodal analysis yields the circuit equations

$$I_1 = \frac{V_1}{10} + \frac{V_1 - V_2}{5} \quad \text{and} \quad I_2 = \frac{V_2}{20} + \frac{V_2 - V_1}{5}. \tag{3.28}$$

That is $$V_1 = (50I_1 + 40I_2)/7 \quad \text{and} \quad V_2 = (40I_1 + 60I_2)/7. \tag{3.29}$$

(a) What is the differential-mode load resistance R_{Ld}?
The differential-mode current $I_d = \frac{1}{2}(I_1 - I_2)$, so, since the common-mode current is zero, set $I_1 = I_d$ and $I_2 = -I_d$ and Equation (3.29) becomes

$$V_1 = \frac{10}{7}I_d, \quad \text{and} \quad V_2 = -\frac{20}{7}I_d. \tag{3.30}$$

The differential-mode voltage is $$V_d = (V_1 - V_2) = \frac{30}{7}I_d. \tag{3.31}$$

Thus $$R_{Ld} = \frac{V_d}{I_d} = \frac{30}{7} = 4.286\ \Omega. \tag{3.32}$$

(b) What is the odd-mode load resistance R_{Lo}?
The odd-mode current $I_o = \frac{1}{2}(I_1 - I_2)$, so set $I_1 = I_o$ and $I_2 = -I_o$ since the common-mode, and hence even-mode, current is zero and Equation (3.29) becomes

$$V_1 = \frac{10}{7}I_o \quad \text{and} \quad V_2 = \frac{-20}{7}I_o. \tag{3.33}$$

The odd-mode voltage is $$V_o = \tfrac{1}{2}(V_1 - V_2) = \frac{30}{14}I_o. \tag{3.34}$$

Thus $$R_{Lo} = \frac{V_o}{I_o} = \frac{30}{14} = 2.143\ \Omega. \tag{3.35}$$

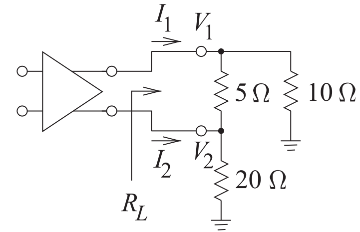


Figure 3-24: A differential amplifier with asymmetrical terminating resistors.

3.6.4 Hybrids and Differential Amplifiers

RFICs use both fully differential and pseudo-differential signal paths. If signal swing is not a concern, a fully-differential signal path is preferred, particularly because of its immunity to noise and its bias stability. The additional transistors involved in realizing a differential circuit (e.g., the current source) reduce the available voltage swing, and hence the power-handling capability. Pseudo-differential signaling uses, in effect, two parallel paths, each referred to ground, but of opposite polarity. The signal on one of the parallel paths is the mirror image of the signal on the other (i.e., the signal is not truly differential, which would imply that it was floating or independent of ground). Each of the parallel paths is unbalanced, but together their RF signal appears to be balanced, or pseudo-balanced. Another consideration is that in working with RFICs it is necessary to interface (unbalanced) microstrip circuits with the inputs and outputs of RFICs. The functionality here requires that signals be split and combined, and converted between balanced and unbalanced signals.

An FDA is shown in Figure 3-25(a). Both the input voltage, $V_i = V_+ - V_-$, and the output voltage, V_o, are differential. Figure 3-25(b and c) show a transformer being used to convert the differential output of the amplifier to an unbalanced signal that, for example, can be connected to a microstrip circuit. The output of many RFICs is pseudo-differential, as this signaling provides large voltage swings. A pseudo-differential amplifier is shown in Figure 3-25(d), but before dealing with manipulation of the signal path, first consider the hybrid on its own.

Figure 3-26(a) shows how two pseudo-balanced signals can be combined to yield a single balanced signal. This $180°$ hybrid function is realized by a **center-tapped transformer**. The signal at Terminal 2 is referenced to ground, and these two terminals are Port 2. The image component of the pseudo-differential signal is applied to Port 3, comprising Terminal 3 and ground. The balanced signal at Port 1 can be directly connected to a microstrip line that is, of course, unbalanced. Most implementations of hybrids at microwave frequencies have ports that are referenced to ground. This is emphasized in Figure 3-26(b), making it easier to see how a $180°$ hybrid can be used to combine a pseudo-differential signal, as shown in Figure 3-26(c). This pseudo-differential-to-unbalanced interface is shown in Figure 3-25(e–g) with a pseudo-differential amplifier.

Hybrids can be used at the input and output terminals of an RFIC pseudo-differential amplifier so that an unbalanced source can efficiently drive the RFIC and then the output of the RFIC can be converted to an unbalanced port to interface with unbalanced circuitry, such as filters and transmission lines. In the RFIC-based system in Figure 3-27, a $180°$ hybrid is first used as a **splitter** and then at the output as a **combiner**.

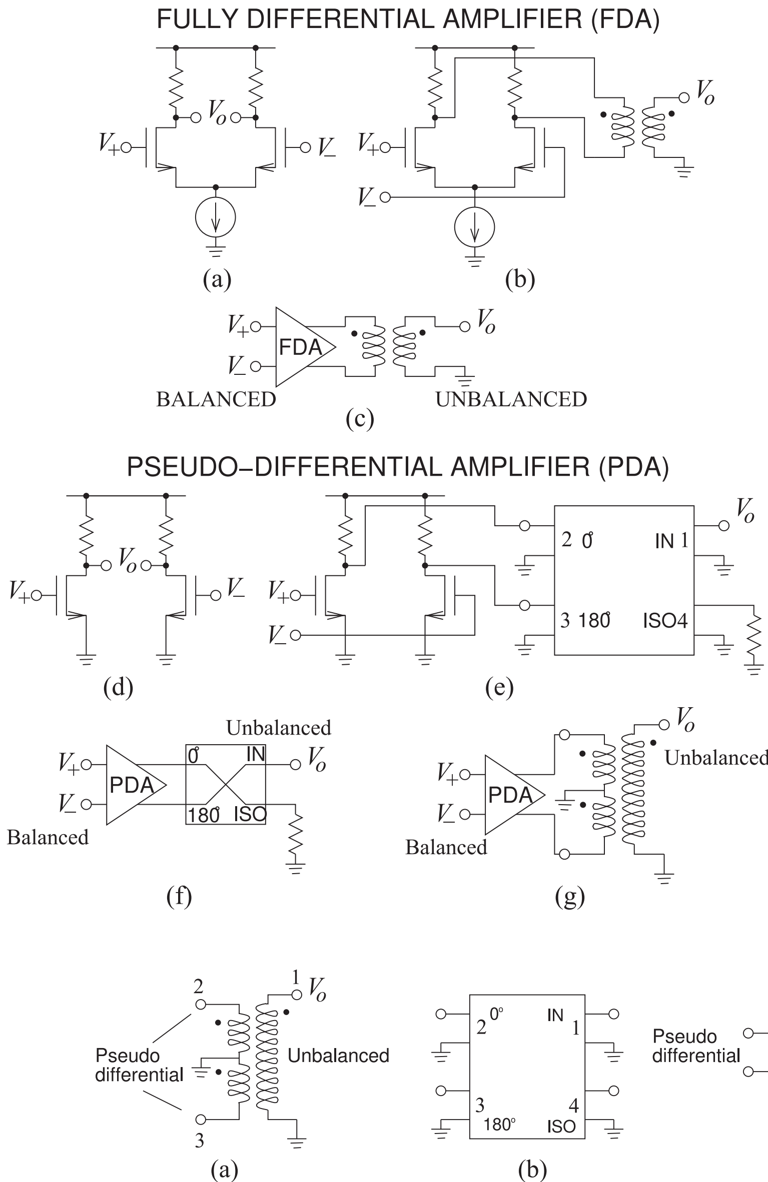


Figure 3-25: Configurations providing an unbalanced output from a differential amplifier: (a) FDA; (b) FDA configured with a balun; (c) schematic; (d) PDA; (e) PDA configured with a 180° hybrid to provide an unbalanced output; (f) schematic; and (g) PDA with a transformer connection yielding an unbalanced output.

Figure 3-26: Equivalent representations of a 180° hybrid connected to provide an interface between a pseudo-differential balanced port and an unbalanced port: (a) a transformer configured as a 180° hybrid with pseudo-unbalanced-to-balanced configuration; (b) hybrid showing two terminal representation of ports; and (c) schematic of a 180° hybrid with the isolation port terminated in a matched load.

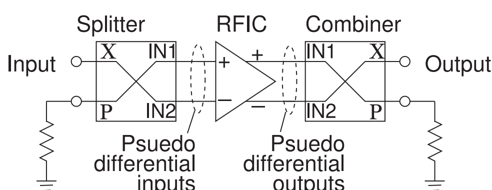


Figure 3-27: An RFIC with differential inputs and outputs driven by a 180° hybrid used as a splitter and followed by another 180° hybrid used as a combiner.

3.7 Case Study: Distributed Biasing of a Pseudo-Differential Amplifier

In this case study a broadband distributed balun-like section is presented as an alternative to inductor-biasing of a pseudo-differential amplifier (PDA). The distributed biasing circuit discriminates between differential- and common-mode signals, resulting in rejection of common-mode signals. A PDA is shown in Figure 3-28, where the inductors present high RF impedances to the transistors while providing low-impedance paths for bias currents. However, inductive biasing of pseudo-differential circuits presents the same environment to common- and differential-mode signals so that the CMRR is 1.

Differential amplifiers have large differential gain, A_d. At the same time it is desirable to minimize the common-mode gain, A_c, as the resulting high CMRR provides immunity to substrate-induced noise. Considering that each transistor has transconductance, g_m, and that even- and odd-mode impedances, Z_{EVEN} and Z_{ODD}, are presented to the drains of the transistors, then the gains are approximately

$$A_d = g_m Z_{\text{ODD}} \text{ and } A_c = g_m Z_{\text{EVEN}}, \tag{3.36}$$

and so $$\text{CMRR} = A_d/A_c = Z_{\text{ODD}}/Z_{\text{EVEN}}. \tag{3.37}$$

The desired amplifier characteristics are thus obtained by synthesizing the even- and odd-mode impedances.

First consider the inductively biased circuit in Figure 3-28. Modal analysis of the inductor biasing circuit results in the circuit model shown in Figure 3-29, from which the total even-mode impedance is

$$Z_{\text{EVEN}}(s) = (sL + R_{DD}/2)\,//R_L, \tag{3.38}$$

where // indicates a parallel connection, and the total odd-mode impedance is

$$Z_{\text{ODD}}(s) = sL//R_L. \tag{3.39}$$

Since R_{DD} is usually negligible and L is a bias or choke inductor so that sL is very large, $Z_{\text{ODD}} \approx R_D \approx Z_{\text{EVEN}}$ and so the CMRR is 1. However, a coupled-line network can provide different model impedances.

Now consider the Marchand balun-like structure in Figure 3-30 that replaces the drain bias circuit in Figure 3-28. The Marchand Balun structure

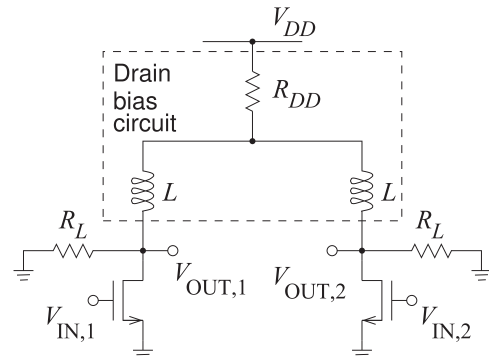


Figure 3-28: A PDA amplifier with bias inductors, L, at the drains, parasitic supply resistance, R_{DD}, and single-ended load impedance, R_L. L is also known as a choke inductor chosen so that its impedance is very large at the maximum operating frequency, i.e. $|sL| \gg R_L$.

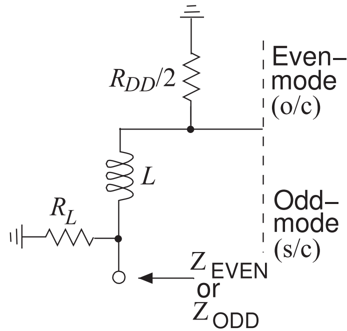


Figure 3-29: Modal subcircuits of the inductor-based biasing circuit of Figure 3-28, including single-ended load resistance R_L.

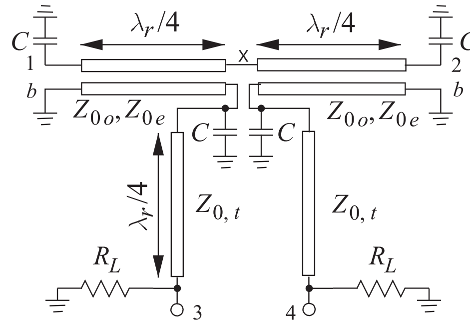


Figure 3-30: Marchand balun-like biasing circuit with single-ended load resistance R_L. External DC bias is applied at Ports b using decoupling capacitors to ensure RF ground.

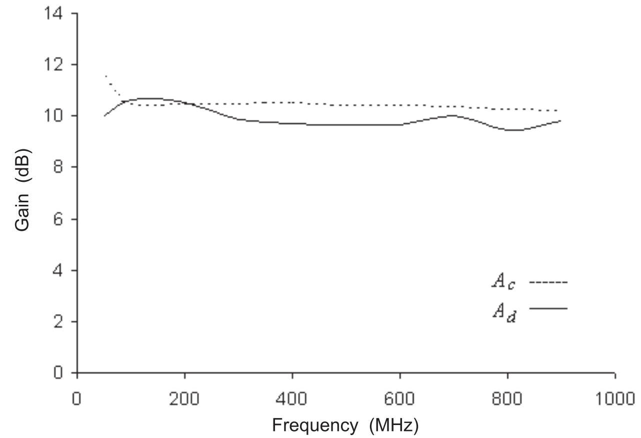
presents different impedances for common- and differential-mode signals. The synthesis of this biasing circuit is described in [8, 9] and follows a procedure similar to that for filter design. So high CMRR performance is the result of presenting different even- and odd-mode impedances to the active devices. The final results of the design are shown in Figure 3-31, first for inductive-biasing of the PDA and then for the coupled-line balun-like biasing circuit.

3.8 Amplifiers and RFICs

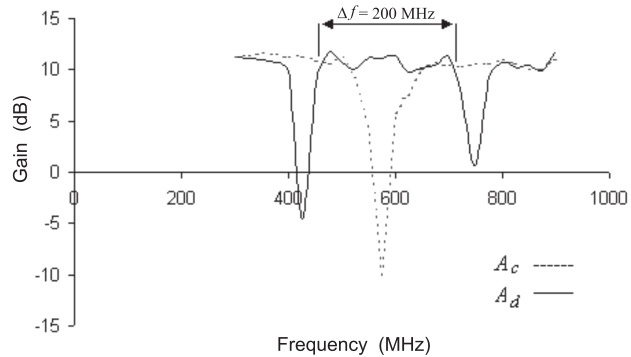
Silicon RFICs exploit the high-density integration possible with silicon MOSFET transistors. These transistors can be fabricated with high levels of repeatability so that the transistors in differential designs can be closely matched. As well, the inherent compatibility with digital circuits enables digital control of RF circuits. As far as amplifiers are concerned, there are a few commonly used basic circuits that use complementary MOSFETs (nMOS and pMOS), that is, CMOS transistors. MOSFET differential amplifiers have been presented throughout this chapter. Other common CMOS circuits are shown in Figure 3-32. The transistors in all the circuits described here operate in the saturation region.

A **cascode amplifier** is shown in Figure 3-32(a). There are two FETs, with the top FET acting as the drain load of the bottom FET. The gate of the top FET is held at ground so the voltage at the source of the top FET (and the drain of the bottom FET) is held at a nearly constant voltage. Thus the top FET presents a low-resistance load to the bottom FET. The voltage gain of the bottom FET is low, and this reduces the **Miller effect capacitance**, which is the effective input capacitance (being the gate-drain capacitance multiplied by the transistor voltage gain). The cascode topology increases the bandwidth of the circuit. Current gain, and hence power gain, is still realized by the bottom transistor. The voltage gain of the circuit depends on the resistance presented to the drain of the top transistor.

A variable gain **cascode amplifier** is shown in Figure 3-32(b). This is similar to the cascode amplifier of Figure 3-32(a), but now the voltage at



(a)



(b)

Figure 3-31: Measured common-mode gain, A_c, and differential-mode gain, A_d: (a) with inductor-based biasing circuit with lumped inductors of 0.75 μH; and (b) with balun-like biasing circuit without lumped capacitors.

the gate of the top transistor, V_{G1}, is selected so that a variable resistance is presented to the bottom transistor, thus the voltage gain of the circuit can be varied. This is a variable gain amplifier.

FET circuits are nearly always current biased, so circuits that realize current sources and current matching are particularly important. A single MOSFET can be used to realize a current source. If the gate-to-source voltage of a MOSFET is fixed, a near-constant current source is realized (see the drain-source current equation, Equation (1.17)). A differential amplifier circuit with a variable current source is shown in Figure 3-32(d). What is particularly interesting is that the transistor controlling the bias to the current source can be part of a digital circuit, enabling digital control of the analog circuit bias. The concept can be replicated by replacing M_1 by multiple transistors in parallel with each transistor having a binary signal at the gate. This is a fundamental component in the **digital control** of analog circuits, including RFICs. For example, modern RFICs incorporate digitally controlled trimming of RFICs to achieve, for example, enhanced IQ balance of quadrature modulators.

Another circuit that controls current in an RFIC is the **current mirror** shown in Figure 3-32(c). In this circuit, $I_1 = I_2$, as the gate-source voltages of transistors M_1 and M_2 are the same. The drain-gate connection of M_1 ensures

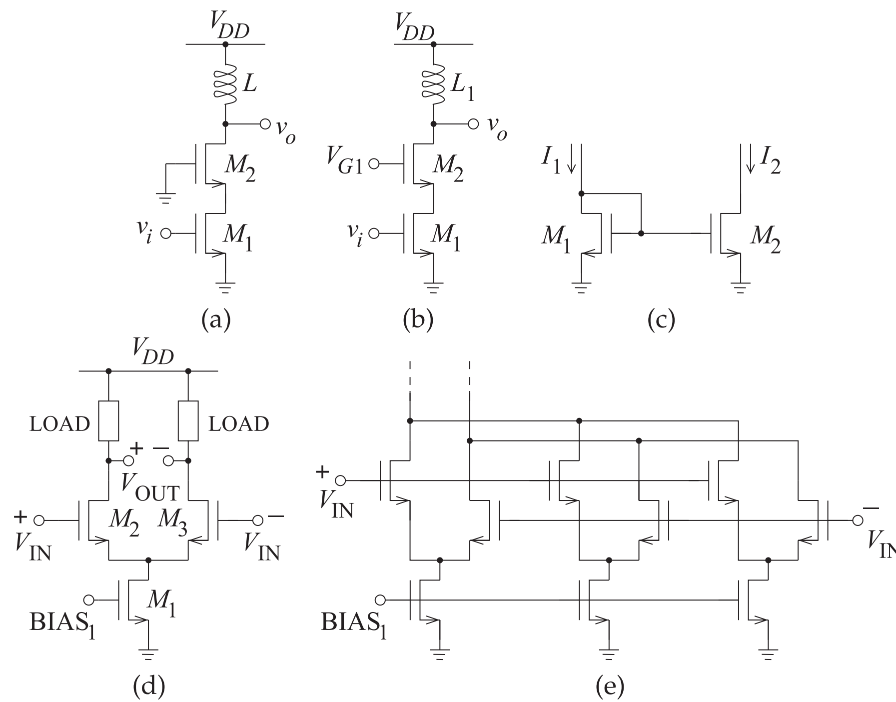
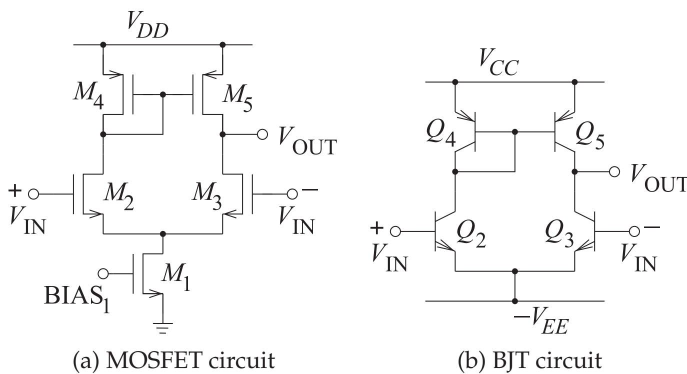


Figure 3-32: MOS analog circuits: (a) cascode amplifier; (b) variable gain cascode amplifier; (c) current mirror; (d) differential pair; (e) multi-tanh triplet implementation of a differential pair providing enhanced linearity.



(a) MOSFET circuit (b) BJT circuit

Figure 3-33: Differential pair circuits each with a current mirror.

that the gate-source voltage will be whatever is needed to support the current I_1 derived from the rest of the circuit.

A CMOS differential amplifier with a current mirror load is shown in Figure 3-33(a). In this configuration the current mirror presents a high differential impedance. If the load impedance presented to the terminal, labeled V_{OUT}, is less than this load, then the current mirror-loaded differential amplifier realizes a single-ended output while having the essential functionality of a differential circuit to reject common-mode signals. There is a price to pay for this functionality. The circuit of Figure 3-33(a) has three drain-source voltage drops between the rails. This reduces the available

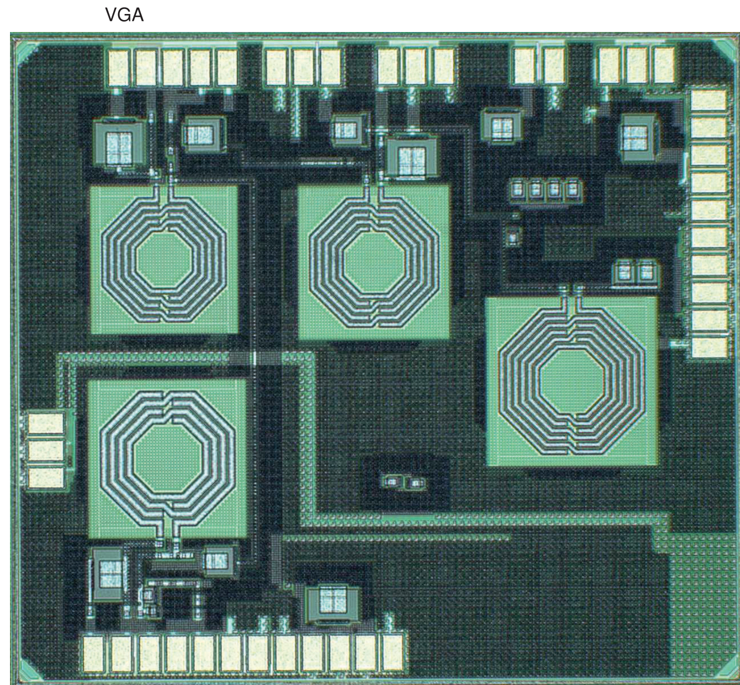


Figure 3-34: Photomicrograph of a 90 nm CMOS WCDMA transmitter showing (MIXER) the up-conversion mixer and quadrature LO divider; (VGA) the cascode variable gain amplifier; and the two-stage driver amplifier with 9.6 dBm output power. Die size is 1.1 mm × 1.4 mm. After Yang [21], and Yang and Gard [12]. Copyright K. Gard and X. Yang, used with permission.

voltage swing. This is one of the major problems encountered with RFICs, as the supply voltage is dictated by the relatively low supply voltages that can be supported in a process that is optimized for low-voltage digital circuits. A current mirror can also be realized using BJTs with the BJT-based current mirror-loaded differential pair shown in Figure 3-33(b) as an example.

Mathematically the simplified input-output characteristic of a MOSFET is essentially a quadratic (see Equation (1.17)). It is a challenge to take such fundamental algebraic models and derive the equations that describe the operation of a complete circuit; a challenge that must be addressed in the synthesis of a circuit with specified distortion and noise performance. It can be shown that the relationship between the drain current and the drain-source voltage has the form of a tanh function [10]. In terms of the transconductance, g_m, it appears as a quadratic-like function with a peak value at a drain voltage that is controlled by the W/L ratio. By putting several differential pairs in parallel, with each pair having staggered W/L ratios, a compound differential amplifier with enhanced linearity can be realized [11, 12]. This circuit is known as a multi-tanh differential pair. A triplet **multi-tanh differential pair** is shown in Figure 3-32(e). Detailed RFIC design involves the algebraic derivation of the required conditions. This network synthesis applied to RFICs is explored in numerous references [13–20] as well as a large number of papers on RFIC design. Synthesis to control distortion and noise is at the heart of RFIC design. Collecting novel circuit topologies, and the techniques to synthesize them (e.g. from conference and journal papers and patents), is an essential part of RFIC design; which is not that different from the process for all other forms of circuit design.

Figure 3-34 is a photomicrograph of a 90 nm WCDMA transmitter. The design consists of three blocks: an up-converting mixer (MIXER), a variable gain cascode amplifier (VGA), and a two-stage driver amplifier. The

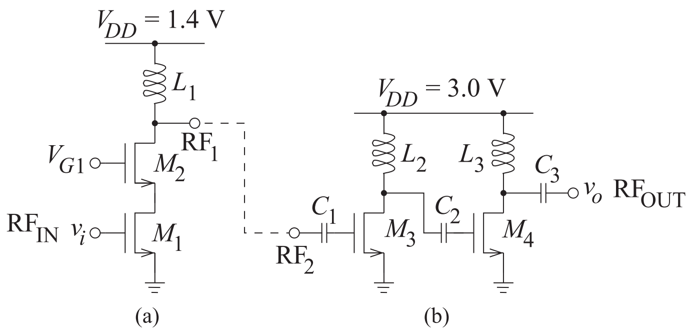


Figure 3-35: Three-stage amplifier of the WCDMA receiver shown in Figure 3-34: (a) a variable gain cascode amplifier; and (b) the two-stage driver amplifier. After Yang [21], and Yang and Gard [12]. Copyright K. Gard and X. Yang, used with permission.

schematic of the output amplifier stages is shown in Figure 3-35. The variable gain amplifier, the VGA block, is a cascode amplifier with variable biasing of the top FET in the cascode to realize a variable gain. Each of the amplifiers in the two-stage driver amplifier has a different V_{DD} so that the nonlinearities of the two stages can be designed to cancel, and thus the overall performance of the driver amplifier is linearized [12, 21].

3.9 Summary

The bandwidth of an amplifier is limited by both the frequency-dependent transconductance of the active device and by the device parasitics. The frequency-dependent transconductance is most significant with FETs as the basic operating control mechanism at the gate is the field produced at a capacitor. Thus the transconductance of a FET varies as the inverse of frequency. With unpackaged transistors, the device parasitics are capacitors. These are augmented by inductances and transmission line effects in packaged devices. Also the feedback capacitor between the collector/drain and base/gate becomes important at higher frequencies. Ignoring the feedback capacitance and thinking just about the input of the transistor, the input of the transistor is a capacitance sometimes in series and sometimes in parallel with a resistance, with the resistance describing the absorption of RF input power by the transistor.

There are two main approaches to wideband amplifier design. One is the synthesis of a matching network that provides a match over a bandwidth that is rarely more than one-half octave wide at microwave frequencies. One way of visualizing the design difficulty is to realize that a simple circuit comprising a resistor and a capacitor (this could represent the input and output equivalent circuits of an active deice) have a locus with respect to frequency that rotates clockwise on a Smith chart. Matching requires that the complex conjugate of the impedance be matched, so matching network design requires that a circuit be synthesized that has a counterclockwise rotation on the Smith chart. Such a circuit can be realized using a transmission line network, but matches over one-half octave of bandwidth are usually all that can be achieved. Another approach to wideband amplifier design is to use multiple active devices and incorporate the device parasitics into input and output transmission lines. This distributed amplifier approach can realize amplifier bandwidths of two or more octaves.

A third approach, which was considered through a case study, is to consider the design problem as a filter synthesis problem. Indeed, following the active device directly with a filter and bypassing the matching network

can broaden the amplifier bandwidth by eliminating the bandwidth limiting effect of matching to a specific system impedance. The necessary impedance transformation is performed in the filter. That is, the doubly terminated filter network has one impedance at the first port (e.g., the lower output impedance of the amplifier) and another impedance, say the system impedance, at the second port.

3.10 References

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3.11 Exercises

1. Consider a $Z_0 = 50\,\Omega$ transmission line of length $\lambda/10$ at 30 GHz.
   (a) Calculate the $ABCD$ parameters of the transmission line at 30 GHz?
   (b) With the transmission line shunted by 0.05 pF capacitors at each end, calculate the $ABCD$ parameters of the augmented transmission line.
   (c) At 30 GHz the augmented transmission line is equivalent to a single transmission line with characteristic impedance Z_{01} and length ℓ_1. What is ℓ_1 in terms of wavelengths?
   (d) What is Z_{01}?
2. A four-stage distributed FET amplifier as shown in Figure 3-1 has $R_S = R_L = 50\,\Omega$. If the capacitive and resistive loading of the transistors are ignored, what are the optimum values of R_1 and R_2? Provide your reasoning.
3. The four-stage distributed FET amplifier shown in Figure 3-1 has $R_S = 80\,\Omega$ and $R_L = 25\,\Omega$. If the capacitive and resistive loading of the transistors are ignored, what are the optimum values of R_1 and R_2? Provide your reasoning.
4. The input matching network of the wideband amplifier considered in Section 3.5 is shown in Figure 3-13(b). (Note that Port 2 of the input network is connected to the transistor.) Typically the complex conjugate of S_{22} of the input network would match the input reflection coefficient, $\Gamma_{\rm in}$, of the transistor. Put your answers in magnitude-angle form.
   (a) Draw the input matching network showing where S_{22} is determined. Also draw the transistor terminated by the output matching network and indicate where $\Gamma_{\rm in}$ is calculated.
   (b) Use a microwave simulator to calculate the S_{22} of the input matching network at 8, 9, . . ., 12 GHz.
   (c) Determine S_{22}^* of the input matching network at 8, 9, . . ., 12 GHz.
   (d) Determine S_{11} of the transistor at 8, 9, . . ., 12 GHz.
   (e) Determine $\Gamma_{\rm in}$ of the transistor (terminated in the output matching network) at 8, 9, . . ., 12 GHz.
   (f) On a Smith chart plot S_{22}^* of the input network, S_{11} of the transistor, and $\Gamma_{\rm in}$ of the transistor.
   (g) Describe the input matching network condition for maximum power transfer used in narrowband amplifier design.
   (h) Discuss the mismatch of $\Gamma_{\rm in}$ of the transistor and S_{22}^* of the input matching network. Describe the effect that this has on the broadband response of the amplifier.
5. The output matching network of the wideband amplifier considered in Section 3.5 is shown in Figure 3-14(b). (Note that Port 2 of the input network is connected to the transistor.) Typically the complex conjugate of S_{22} of the output network would match the input reflection coefficient, $\Gamma_{\rm out}$, of the transistor. Put your answers in magnitude-angle form.
   (a) Draw the output matching network showing where S_{22} is determined. Also draw the transistor terminated by the input matching network and indicate where $\Gamma_{\rm out}$ is calculated.
   (b) Use a microwave simulator to calculate the S_{22} of the output matching network at 8, 9, . . ., 12 GHz.
   (c) Determine S_{22}^* of the output matching network at 8, 9, . . ., 12 GHz.
   (d) Determine S_{22} of the transistor at 8, 9, . . ., 12 GHz.
   (e) Determine $\Gamma_{\rm out}$ of the transistor (terminated in the output matching network) at 8, 9, . . ., 12 GHz.
   (f) On a Smith chart plot S_{22}^* of the output network, S_{22} of the transistor, and $\Gamma_{\rm out}$ of the transistor.
   (g) Describe the output matching network condition for maximum power transfer used in narrowband amplifier design.
   (h) Discuss the mismatch of $\Gamma_{\rm out}$ of the transistor and S_{22}^* of the output matching network. Describe the effect that this has on the broadband response of the amplifier. You will want to consider the S_{21} of the transistor.
6. Plot the 50 Ω S_{11} and S_{22} parameters from 8 GHz to 12 GHz of the wideband amplifier considered in Section 3.5. It will be seen that the amplifier is not matched across the band. Discuss the reason why there is a mismatch even though the gain and noise figure of the amplifier, shown in Figure 3-18, are relatively flat from from 8 GHz to 12 GHz. Note that Port 1 is the input port of the amplifier and Port 2 is the output Port.
7. The output of a transistor is modeled as the shunt connection of a current source, a 20 Ω re-